



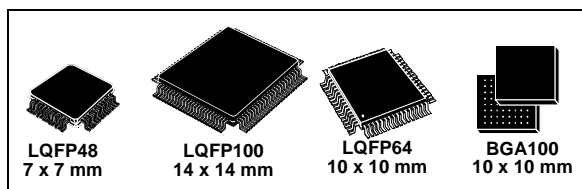
# STM32F103x6 STM32F103x8 STM32F103xB

Performance line, ARM-based 32-bit MCU with Flash, USB, CAN, seven 16-bit timers, two ADCs and nine communication interfaces

Preliminary Data

## Features

- Core: ARM 32-bit Cortex™-M3 CPU
  - 72 MHz, 90 DMIPS with 1.25 DMIPS/MHz
  - Single-cycle multiplication and hardware division
  - Nested interrupt controller with 43 maskable interrupt channels
  - Interrupt processing (down to 6 CPU cycles) with tail chaining
- Memories
  - 32-to-128 Kbytes of Flash memory
  - 6-to-20 Kbytes of SRAM
- Clock, reset and supply management
  - 2.0 to 3.6 V application supply and I/Os
  - POR, PDR, and programmable voltage detector (PVD)
  - 4-to-16 MHz quartz oscillator
  - Internal 8 MHz factory-trimmed RC
  - Internal 32 kHz RC
  - PLL for CPU clock
  - Dedicated 32 kHz oscillator for RTC with calibration
- Low power
  - Sleep, Stop and Standby modes
  - $V_{BAT}$  supply for RTC and backup registers
- 2 x 12-bit, 1  $\mu$ s A/D converters (16-channel)
  - Conversion range: 0 to 3.6 V
  - Dual-sample and hold capability
  - Synchronizable with advanced control timer
  - Temperature sensor
- DMA
  - 7-channel DMA controller
  - Peripherals supported: timers, ADC, SPIs, I<sup>2</sup>Cs and USARTs



- Debug mode
  - Serial wire debug (SWD) & JTAG interfaces
- Up to 80 fast I/O ports
  - 32/49/80 5 V-tolerant I/Os
  - All mappable on 16 external interrupt vectors
  - Atomic read/modify/write operations
- Up to 7 timers
  - Up to three 16-bit timers, each with up to 4 IC/OC/PWM or pulse counter
  - 16-bit, 6-channel advanced control timer:
    - up to 6 channels for PWM output
    - Dead time generation and emergency stop
  - 2 x 16-bit watchdog timers (Independent and Window)
  - SysTick timer: a 24-bit downcounter
- Up to 9 communication interfaces
  - Up to 2 x I<sup>2</sup>C interfaces (SMBus/PMBus)
  - Up to 3 USARTs (ISO 7816 interface, LIN, IrDA capability, modem control)
  - Up to 2 SPIs (18 Mbit/s)
  - CAN interface (2.0B Active)
  - USB 2.0 full speed interface

Table 1. Device summary

Reference	Root part number
STM32F103x6	STM32F103C6, STM32F103R6
STM32F103x8	STM32F103C8, STM32F103R8 STM32F103V8
STM32F103xB	STM32F103RB STM32F103VB

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# 1 Introduction

This datasheet provides the STM32F103xx performance line ordering information and mechanical device characteristics.

For information on programming, erasing and protection of the internal Flash memory please refer to the *STM32F10xxx Flash programming reference manual*, pm0042, available from [www.st.com](http://www.st.com).

For information on the Cortex-M3 core please refer to the Cortex-M3 Technical Reference Manual.

# 2 Description

The STM32F103xx performance line family incorporates the high-performance ARM Cortex-M3 32-bit RISC core operating at a 72 MHz frequency, high-speed embedded memories (Flash memory up to 128Kbytes and SRAM up to 20 Kbytes), and an extensive range of enhanced I/Os and peripherals connected to two APB buses. All devices offer two 12-bit ADCs, three general purpose 16-bit timers plus one PWM timer, as well as standard and advanced communication interfaces: up to two I<sup>2</sup>Cs and SPIs, three USARTs, an USB and a CAN.

The STM32F103xx performance line family operates in the -40 to +105 °C temperature range, from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving mode allows to design low-power applications.

The complete STM32F103xx performance line family includes devices in 4 different package types: from 48 pins to 100 pins. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

These features make the STM32F103xx performance line microcontroller family suitable for a wide range of applications:

- Motor drive and application control
- Medical and handheld equipment
- PC peripherals gaming and GPS platforms
- Industrial applications: PLC, inverters, printers, and scanners
- Alarm systems, Video intercom, and HVAC

*Figure 1* shows the general block diagram of the device family.



## 2.1 Device overview

Table 2. Device features and peripheral counts (STM32F103xx performance line)

Peripheral		STM32F103Cx		STM32F103Rx			STM32F103Vx	
Flash - Kbytes		32	64	32	64	128	64	128
SRAM - Kbytes		10	20	10	20		20	
Timers	General purpose	2	3	2	3		3	
	Advanced Control	1		1			1	
Communication	SPI	1	2	1	2		2	
	I <sup>2</sup> C	1	2	1	2		2	
	USART	2	3	2	3		3	
	USB	1	1	1	1		1	
	CAN	1	1	1	1		1	
GPIOs		32		49			80	
12-bit synchronized ADC Number of channels		2 10 channels		2 16 channels				
CPU frequency		72 MHz						
Operating voltage		2.0 to 3.6 V						
Operating temperature		-40 to +85 °C / -40 to +105 °C						
Packages		LQFP48		LQFP64			LQFP100, BGA100	

## 2.2 Overview

### ARM® Cortex™-M3 core with embedded Flash and SRAM

The ARM Cortex-M3 processor is the latest generation of ARM processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM Cortex-M3 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The STM32F103xx performance line family having an embedded ARM core, is therefore compatible with all ARM tools and software.

*Figure 1* shows the general block diagram of the device family.

### Embedded Flash memory

- Up to 128 Kbytes of embedded Flash is available for storing programs and data.

### Embedded SRAM

Up to 20 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states.

### Nested vectored interrupt controller (NVIC)

The STM32F103xx performance line embeds a Nested Vectored Interrupt Controller able to handle up to 43 maskable interrupt channels (not including the 16 interrupt lines of Cortex-M3) and 16 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving* higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

### External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 19 edge detectors lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect external line with pulse width lower than the Internal APB2 clock period. Up to 80 GPIOs are connected to the 16 external interrupt lines.



## Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-16 MHz clock can be selected and is monitored for failure. During such a scenario, it is disabled and software interrupt management follows. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example with failure of an indirectly used external oscillator).

Several prescalers allow the configuration of the AHB frequency, the High Speed APB (APB2) and the low Speed APB (APB1) domains. The maximum frequency of the AHB and the High Speed APB domains is 72 MHz. The maximum allowed frequency of the Low Speed APB domain is 36 MHz.

## Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from User Flash
- Boot from System Memory
- Boot from SRAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using the USART.

## Power supply schemes

- $V_{DD} = 2.0$  to  $3.6$  V: external power supply for I/Os and the internal regulator. Provided externally through  $V_{DD}$  pins.
- $V_{SSA}$ ,  $V_{DDA} = 2.0$  to  $3.6$  V: external analog power supplies for ADC, Reset blocks, RCs and PLL. In  $V_{DD}$  range (ADC is limited at  $2.4$  V).
- $V_{BAT} = 1.8$  to  $3.6$  V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when  $V_{DD}$  is not present.

## Power supply supervisor

The device has an integrated Power On Reset (POR)/Power Down Reset (PDR) circuitry. It is always active, and ensures proper operation starting from/down to 2 V. The device remains in reset mode when  $V_{DD}$  is below a specified threshold,  $V_{POR/PDR}$ , without the need for an external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the  $V_{DD}$  power supply and compares it to the  $V_{PVD}$  threshold. An interrupt can be generated when  $V_{DD}$  drops below the  $V_{PVD}$  and/or when  $V_{DD}$  is higher than the  $V_{PVD}$  threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

Refer to [Table 9: Embedded reset and power control block characteristics](#) for the values of  $V_{POR/PDR}$  and  $V_{PVD}$ .

### Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR) and power down.

- MR is used in the nominal regulation mode (Run)
- LPR is used in the Stop modes.
- Power down is used in Standby Mode: the regulator output is in high impedance: the kernel circuitry is powered-down, inducing zero consumption (but the contents of the registers and SRAM are lost)

This regulator is always enabled after reset. It is disabled in Standby Mode, providing high impedance output.

### Low-power modes

The STM32F103xx performance line supports three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop mode**

Stop mode allows to achieve the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI and the HSE RC oscillators are disabled. The voltage regulator can also be put either in normal or in low power mode.

The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm or the USB wakeup.

- **Standby mode**

The Standby mode allows to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI and the HSE RC oscillators are also switched off. After entering Standby mode, SRAM and registers content are lost except for registers in the Backup domain and Standby circuitry.

The device exits Standby mode when an external reset (NRST pin), a IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

*Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.*

### DMA

The flexible 7-channel general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I<sup>2</sup>C, USART, general purpose and advanced control timers TIMx and ADC.

### RTC (real-time clock) and backup registers

The RTC and the backup registers are supplied through a switch that takes power either on  $V_{DD}$  supply when present or through the  $V_{BAT}$  pin. The backup registers (ten 16-bit registers) can be used to store data when  $V_{DD}$  power is not present.

The real-time clock provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and a periodic interrupt. It is clocked by an external 32.768 kHz oscillator, the internal low power RC oscillator or the High Speed External clock divided by 128. The internal low power RC has a typical frequency of 32 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural quartz deviation. The RTC features a 32-bit programmable counter for long term measurement using the Compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

### Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application time out management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

### Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

### SysTick timer

This timer is dedicated for OS, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

### General purpose timers (TIMx)

There are up to 3 synchronizable standard timers embedded in the STM32F103xx performance line devices. These timers are based on a 16-bit auto-reload up/down counter, a 16-bit prescaler and feature 4 independent channels each for input capture/output compare, PWM or one pulse mode output. This gives up to 12 input captures / output compares / PWMs on the largest packages. They can work together with the Advanced Control Timer via the Timer Link feature for synchronization or event chaining.

The counter can be frozen in debug mode.

Any of the standard timers can be used to generate PWM outputs. Each of the timers has independent DMA request generations.

### Advanced control timer (TIM1)

The advanced control timer (TIM1) can be seen as a three-phase PWM multiplexed on 6 channels. It can also be seen as a complete general-purpose timer. The 4 independent channels can be used for

- Input Capture
- Output Compare
- PWM generation (edge or center-aligned modes)
- One Pulse Mode output
- Complementary PWM outputs with programmable inserted dead-times.

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

The counter can be frozen in debug mode.

Many features are shared with those of the standard TIM timers which have the same architecture. The advanced control timer can therefore work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

### I<sup>2</sup>C bus

Up to two I<sup>2</sup>C bus interfaces can operate in multi-master and slave modes. They can support standard and fast modes.

They support dual slave addressing (7-bit only) and both 7/10-bit addressing in master mode. A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SM Bus 2.0/PM Bus.

### Universal synchronous/asynchronous receiver transmitter (USART)

One of the USART interfaces is able to communicate at speeds of up to 4.5 Mbit/s. The other available interfaces communicate at up to 2.25 Mbit/s. They provide hardware management of the CTS and RTS signals, IrDA SIR ENDEC support, are ISO 7816 compliant and have LIN Master/Slave capability.

All USART interfaces can be served by the DMA controller.

### Serial peripheral interface (SPI)

Up to two SPIs are able to communicate up to 18 Mbits/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable from 8-bit to 16-bit. The hardware CRC generation/verification supports basic SD Card/MMC modes.

Both SPIs can be served by the DMA controller.

### Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

### Universal serial bus (USB)

The STM32F103xx performance line embeds a USB device peripheral compatible with the USB Full-speed 12 Mbs. The USB interface implements a full speed (12 Mbit/s) function interface. It has software configurable endpoint setting and suspend/resume support. The dedicated 48 MHz clock source is generated from the internal main PLL.

### GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current-capable.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

I/Os on APB2 with up to 18 MHz toggling speed

### ADC (analog to digital converter)

Two 12-bit Analog to Digital Converters are embedded into STM32F103xx performance line devices and each ADC shares up to 16 external channels, performing conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold
- Single shunt

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the standard timers (TIMx) and the Advanced Control timer (TIM1) can be internally connected to the ADC start trigger, injection trigger, and DMA trigger respectively, to allow the application to synchronize A/D conversion and timers.

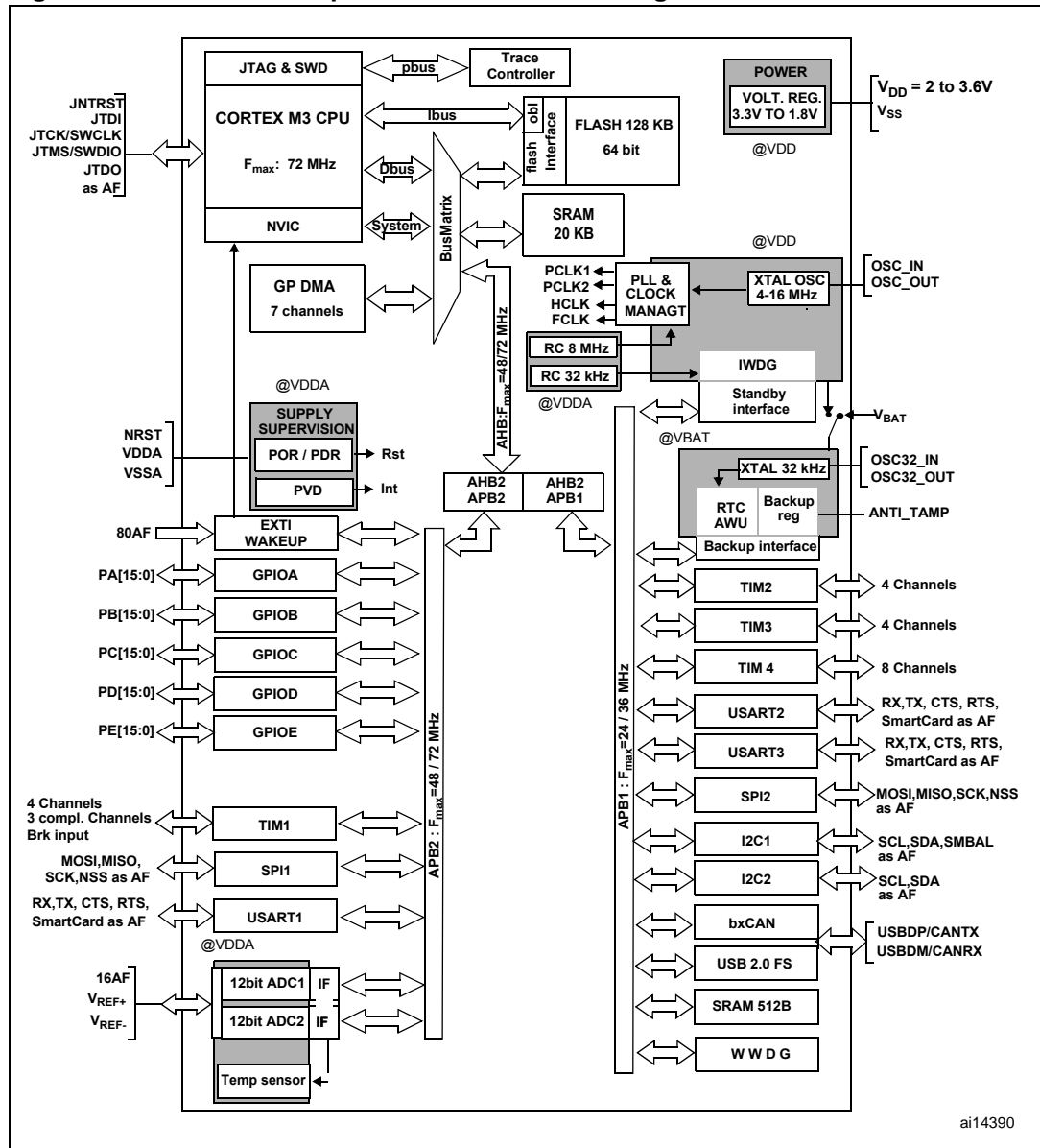
### Temperature sensor

The temperature sensor has to generate a linear voltage with any variation in temperature. The conversion range is between  $2\text{ V} < V_{\text{DDA}} < 3.6\text{ V}$ . The temperature sensor is internally connected to the ADC\_IN16 input channel which is used to convert the sensor output voltage into a digital value.

### Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded. and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

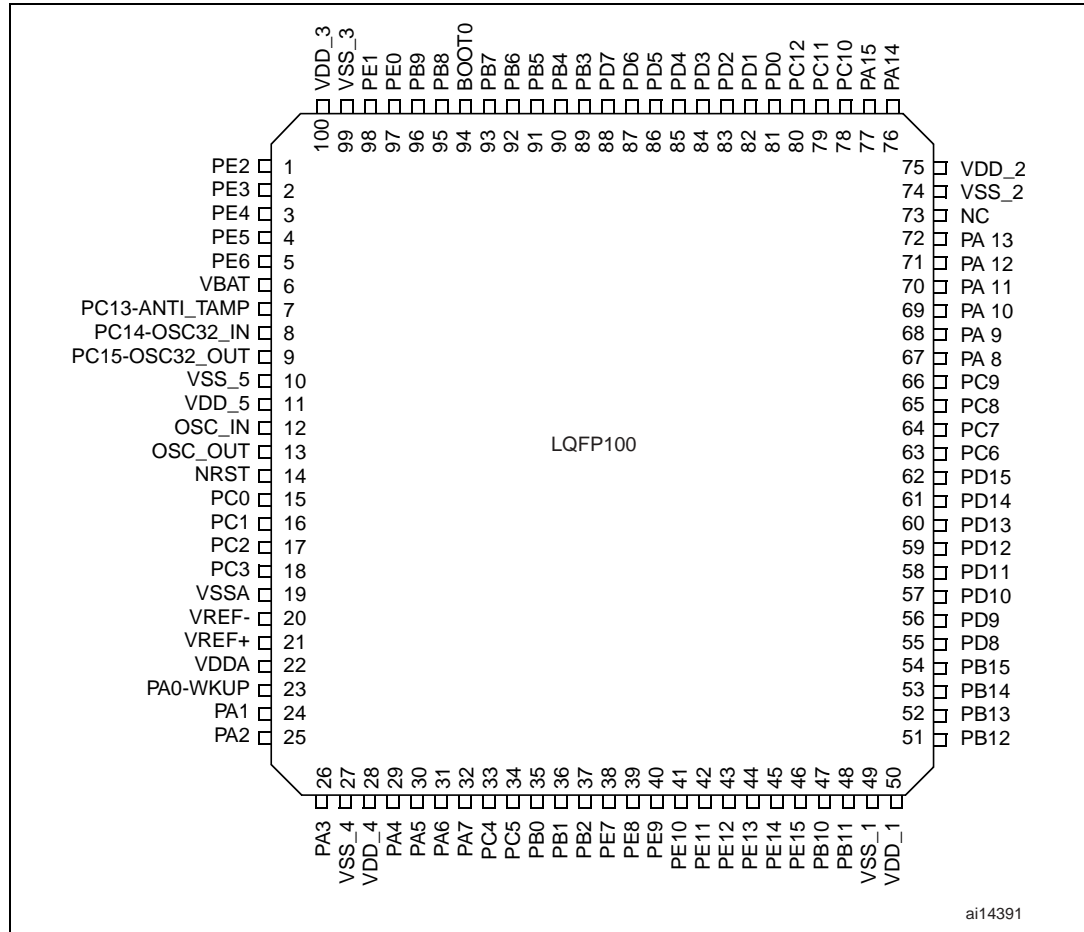
Figure 1. STM32F103xx performance line block diagram



1.  $T_A = -40\text{ }^{\circ}\text{C}$  to  $+105\text{ }^{\circ}\text{C}$  (junction temperature up to  $125\text{ }^{\circ}\text{C}$ ).
2. AF = alternate function on I/O port pin.

### 3 Pin descriptions

Figure 2. STM32F103xx performance line LQFP100 pinout



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Figure 3. STM32F103xx performance line LQFP64 pinout

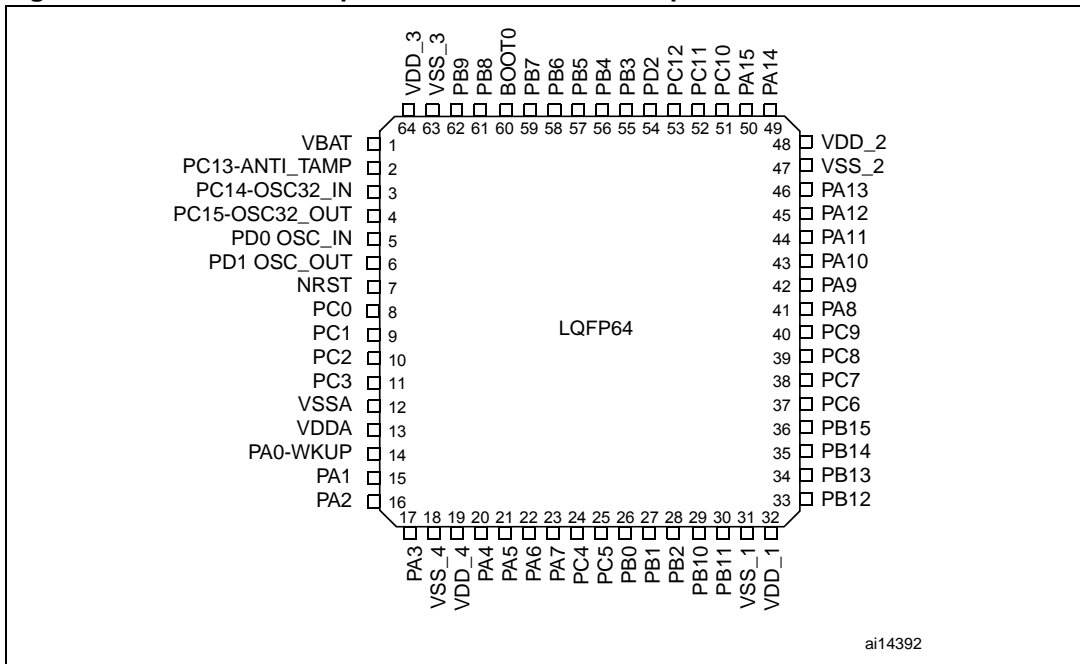


Figure 4. STM32F103xx performance line LQFP48 pinout

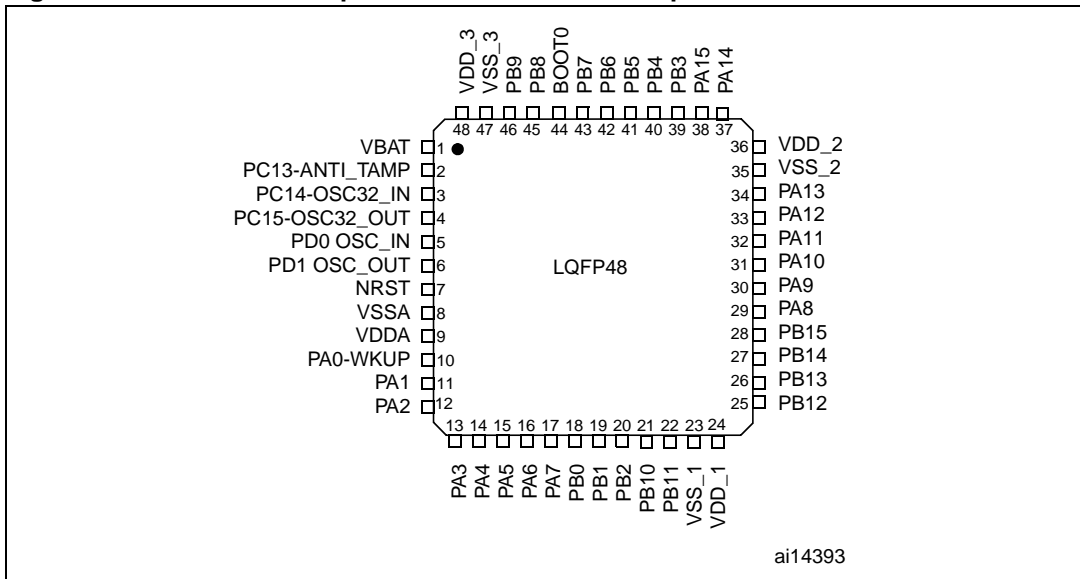




Figure 5. STM32F103xx performance line BGA100 ballout

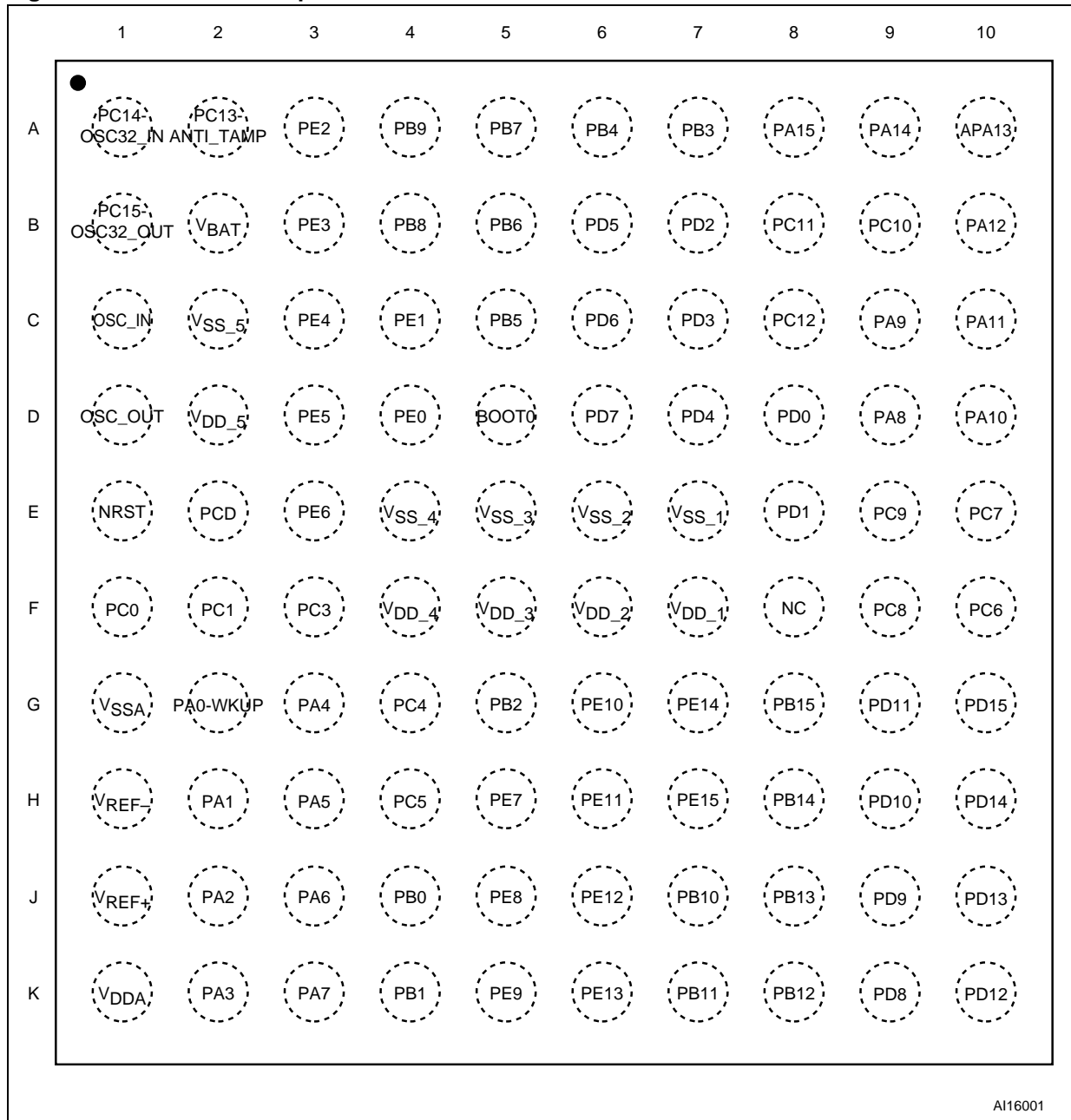


Table 3. Pin definitions

Pins				Pin name	Type <sup>(1)</sup>	I/O Level <sup>(2)</sup>	Main function <sup>(3)</sup> (after reset)	Default alternate functions
BGA100	LQFP48	LQFP64	LQFP100					
A3	-	-	1	PE2/TRACECK	I/O	FT	PE2	TRACECK
B3	-	-	2	PE3/TRACED0	I/O	FT	PE3	TRACED0
C3	-	-	3	PE4/TRACED1	I/O	FT	PE4	TRACED1
D3	-	-	4	PE5/TRACED2	I/O	FT	PE5	TRACED2
E3	-	-	5	PE6/TRACED3	I/O	FT	PE6	TRACED3
B2	1	1	6	V <sub>BAT</sub>	S		V <sub>BAT</sub>	
A2	2	2	7	PC13-ANTI_TAMP <sup>(4)</sup>	I/O		PC13	ANTI_TAMP
A1	3	3	8	PC14-OSC32_IN <sup>(4)</sup>	I/O		PC14-OSC32_IN	
B1	4	4	9	PC15-OSC32_OUT <sup>(4)</sup>	I/O		PC15-OSC32_OUT	
C2	-	-	10	V <sub>SS_5</sub>	S		V <sub>SS_5</sub>	
D2	-	-	11	V <sub>DD_5</sub>	S		V <sub>DD_5</sub>	
C1	5	5	12	OSC_IN	I		OSC_IN	
D1	6	6	13	OSC_OUT	O		OSC_OUT	
E1	7	7	14	NRST	I/O		NRST	
F1	-	8	15	PC0/ADC_IN10	I/O		PC0	ADC_IN10
F2	-	9	16	PC1/ADC_IN11	I/O		PC1	ADC_IN11
E2	-	10	17	PC2/ADC_IN12	I/O		PC2	ADC_IN12
F3	-	11	18	PC3/ADC_IN13	I/O		PC3	ADC_IN13
G1	8	12	19	V <sub>SSA</sub>	S		V <sub>SSA</sub>	
H1	-	-	20	V <sub>REF-</sub>	S		V <sub>REF-</sub>	
J1	-	-	21	V <sub>REF+</sub>	S		V <sub>REF+</sub>	
K1	9	13	22	V <sub>DDA</sub>	S		V <sub>DDA</sub>	
G2	10	14	23	PA0-WKUP/ USART2_CTS/ ADC_IN0/TIM2_CH1_ETR	I/O		PA0	WKUP/USART2_CTS <sup>(6)</sup> /AD C_IN0/ TIM2_CH1_ETR <sup>(6)</sup>
H2	11	15	24	PA1/USART2_RTS/ ADC_IN1/TIM2_CH2	I/O		PA1	USART2_RTS <sup>(6)</sup> / ADC_IN1/ TIM2_CH2 <sup>(6)</sup>
J2	12	16	25	PA2/USART2_TX/ ADC_IN2/TIM2_CH3	I/O		PA2	USART2_TX <sup>(6)</sup> / ADC_IN2/TIM2_CH3 <sup>(6)</sup>
K2	13	17	26	PA3/USART2_RX/ ADC_IN3/TIM2_CH4	I/O		PA3	USART2_RX <sup>(6)</sup> / ADC_IN3/TIM2_CH4 <sup>(6)</sup>
E4	-	18	27	V <sub>SS_4</sub>	S		V <sub>SS_4</sub>	
F4	-	19	28	V <sub>DD_4</sub>	S		V <sub>DD_4</sub>	

Table 3. Pin definitions (continued)

Pins				Pin name	Type <sup>(1)</sup>	I/O Level <sup>(2)</sup>	Main function <sup>(3)</sup> (after reset)	Default alternate functions
BGA100	LQFP48	LQFP64	LQFP100					
G3	14	20	29	PA4/SPI1_NSS/ USART2_CK/ADC_IN4	I/O		PA4	SPI1_NSS <sup>(6)</sup> / USART2_CK <sup>(6)</sup> / ADC_IN4
H3	15	21	30	PA5/SPI1_SCK/ ADC_IN5	I/O		PA5	SPI1_SCK <sup>(6)</sup> / ADC_IN5
J3	16	22	31	PA6/SPI1_MISO/ ADC_IN6/TIM3_CH1	I/O		PA6	SPI1_MISO <sup>(6)</sup> / ADC_IN6/TIM3_CH1 <sup>(6)</sup>
K3	17	23	32	PA7/SPI1_MOSI/ ADC_IN7/TIM3_CH2	I/O		PA7	SPI1_MOSI <sup>(6)</sup> / ADC_IN7/TIM3_CH2 <sup>(6)</sup>
G4	-	24	33	PC4/ADC_IN14	I/O		PC4	ADC_IN14
H4	-	25	34	PC5/ADC_IN15	I/O		PC5	ADC_IN15
J4	18	26	35	PB0/ADC_IN8/ TIM3_CH3	I/O		PB0	ADC_IN8/TIM3_CH3 <sup>(6)</sup>
K4	19	27	36	PB1/ADC_IN9/ TIM3_CH4	I/O		PB1	ADC_IN9/TIM3_CH4 <sup>(6)</sup>
G5	20	28	37	PB2 / BOOT1	I/O	FT	PB2/BOOT1	
H5	-	-	38	PE7	I/O	FT	PE7	
J5	-	-	39	PE8	I/O	FT	PE8	
K5	-	-	40	PE9	I/O	FT	PE9	
G6	-	-	41	PE10	I/O	FT	PE10	
H6	-	-	42	PE11	I/O	FT	PE11	
J6	-	-	43	PE12	I/O	FT	PE12	
K6	-	-	44	PE13	I/O	FT	PE13	
G7	-	-	45	PE14	I/O	FT	PE14	
H7	-	-	46	PE15	I/O	FT	PE15	
J7	21	29	47	PB10/I2C2_SCL/ USART3_TX	I/O	FT	PB10	I2C2_SCL/USART3_TX <sup>(5)(6)</sup>
K7	22	30	48	PB11/I2C2_SDA / USART3_RX	I/O	FT	PB11	I2C2_SDA/ USART3_RX <sup>(5)(6)</sup>
E7	23	31	49	V <sub>SS_1</sub>	S		V <sub>SS_1</sub>	
F7	24	32	50	V <sub>DD_1</sub>	S		V <sub>DD_1</sub>	
K8	25	33	51	PB12/SPI2_NSS / I2C2_SMBAl/ USART3_CK / TIM1_BKIN	I/O	FT	PB12	SPI2_NSS <sup>(5)</sup> /I2C2_SMBAl <sup>(5)</sup> / USART3_CK <sup>(5)(6)</sup> / TIM1_BKIN <sup>(6)</sup>
J8	26	34	52	PB13/SPI2_SCK / USART3_CTS / TIM1_CH1N	I/O	FT	PB13	SPI2_SCK <sup>(5)</sup> / USART3_CTS <sup>(5)(6)</sup> / TIM1_CH1N <sup>(6)</sup>
H8	27	35	53	PB14/SPI2_MISO / USART3_RTS / TIM1_CH2N	I/O	FT	PB14	SPI2_MISO <sup>(5)</sup> /USART3_RTS <sup>(5)(6)</sup> TIM1_CH2N <sup>(6)</sup>

Table 3. Pin definitions (continued)

Pins				Pin name	Type <sup>(1)</sup>	I/O Level <sup>(2)</sup>	Main function <sup>(3)</sup> (after reset)	Default alternate functions	
BGA100	LQFP48	LQFP64	LQFP100						
G8	28	36	54	PB15/SPI2_MOSI TIM1_CH3N	I/O	FT	PB15	SPI2_MOSI <sup>(5)</sup> / TIM1_CH3N <sup>(6)</sup>	
K9	-	-	55	PD8	I/O	FT	PD8		
J9	-	-	56	PD9	I/O	FT	PD9		
H9	-	-	57	PD10	I/O	FT	PD10		
G9	-	-	58	PD11	I/O	FT	PD11		
K10	-	-	59	PD12	I/O	FT	PD12		
J10	-	-	60	PD13	I/O	FT	PD13		
H10	-	-	61	PD14	I/O	FT	PD14		
G10	-	-	62	PD15	I/O	FT	PD15		
F10	-	37	63	PC6	I/O	FT	PC6		
E10		38	64	PC7	I/O	FT	PC7		
F9		39	65	PC8	I/O	FT	PC8		
E9	-	40	66	PC9	I/O	FT	PC9		
D9	29	41	67	PA8/USART1_CK/ TIM1_CH1/MCO	I/O	FT	PA8	USART1_CK/ TIM1_CH1 <sup>(6)</sup> /MCO	
C9	30	42	68	PA9/USART1_TX/ TIM1_CH2	I/O	FT	PA9	USART1_TX <sup>(6)</sup> / TIM1_CH2 <sup>(6)</sup>	
D10	31	43	69	PA10/USART1_RX/ TIM1_CH3	I/O	FT	PA10	USART1_RX <sup>(6)</sup> / TIM1_CH3 <sup>(6)</sup>	
C10	32	44	70	PA11 / USART1_CTS/ CANRX / USBDM/ TIM1_CH4	I/O	FT	PA11	USART1_CTS/ CANRX <sup>(6)</sup> / TIM1_CH4 <sup>(6)</sup> / USBDM	
B10	33	45	71	PA12 / USART1_RTS/ CANTX / USBDP/ TIM1_ETR	I/O	FT	PA12	USART1_RTS/ CANTX <sup>(6)</sup> / TIM1_ETR <sup>(6)</sup> / USBDP	
A10	34	46	72	PA13/JTMS/SWDIO	I/O	FT	JTMS/SWDIO	PA13	
F8	-	-	73	Not connected					
E6	35	47	74	V <sub>SS_2</sub>	S		V <sub>SS_2</sub>		
F6	36	48	75	V <sub>DD_2</sub>	S		V <sub>DD_2</sub>		
A9	37	49	76	PA14/JTCK/SWCLK	I/O	FT	JTCK/SWCLK	PA14	
A8	38	50	77	PA15/JTDI	I/O	FT	JTDI	PA15	
B9	-	51	78	PC10	I/O	FT	PC10		
B8	-	52	79	PC11	I/O	FT	PC11		
C8	-	53	80	PC12	I/O	FT	PC12		

Table 3. Pin definitions (continued)

Pins				Pin name	Type <sup>(1)</sup>	I/O Level <sup>(2)</sup>	Main function <sup>(3)</sup> (after reset)	Default alternate functions
BGA100	LQFP48	LQFP64	LQFP100					
D8	5	5	81	PD0	I/O	FT	OSC_IN <sup>(7)</sup>	
E8	6	6	82	PD1	I/O	FT	OSC_OUT <sup>(7)</sup>	
B7		54	83	PD2/TIM3_ETR	I/O	FT	PD2	TIM3_ETR
C7	-	-	84	PD3	I/O	FT	PD3	
D7	-	-	85	PD4	I/O	FT	PD4	
B6	-	-	86	PD5	I/O	FT	PD5	
C6	-	-	87	PD6	I/O	FT	PD6	
D6	-	-	88	PD7	I/O	FT	PD7	
A7	39	55	89	PB3/JTDO/TRACESWO	I/O	FT	JTDO	PB3/TRACESWO
A6	40	56	90	PB4/JNTRST	I/O	FT	JNTRST	PB4
C5	41	57	91	PB5/I2C1_SMBAI	I/O		PB5	I2C1_SMBAI
B5	42	58	92	PB6/I2C1_SCL/ TIM4_CH1	I/O	FT	PB6	I2C1_SCL <sup>(6)</sup> / TIM4_CH1 <sup>(5)(6)</sup>
A5	43	59	93	PB7/I2C1_SDA/ TIM4_CH2	I/O	FT	PB7	I2C1_SDA <sup>(6)</sup> / TIM4_CH2 <sup>(5)(6)</sup>
D5	44	60	94	BOOT0	I		BOOT0	
B4	45	61	95	PB8/TIM4_CH3	I/O	FT	PB8	TIM4_CH3 <sup>(5)(6)</sup>
A4	46	62	96	PB9/TIM4_CH4	I/O	FT	PB9	TIM4_CH4 <sup>(5)(6)</sup>
D4	-	-	97	PE0/TIM4_ETR	I/O	FT	PE0	TIM4_ETR <sup>(5)</sup>
C4	-	-	98	PE1	I/O	FT	PE1	
E5	47	63	99	V <sub>SS_3</sub>	S		V <sub>SS_3</sub>	
F5	48	64	100	V <sub>DD_3</sub>	S		V <sub>DD_3</sub>	

1. I = input, O = output, S = supply, HiZ = high impedance.

2. FT= 5 V tolerant.

3. Function availability depends on the chosen device. Refer to [Table 2 on page 7](#).

4. PC13, PC14 and PC15 are supplied through the power switch, and so their use in output mode is limited: they can be used only in output 2 MHz mode with a maximum load of 30 pF and only one pin can be put in output mode at a time.

5. Available only on devices with a Flash memory density equal or higher than 64 Kbytes.

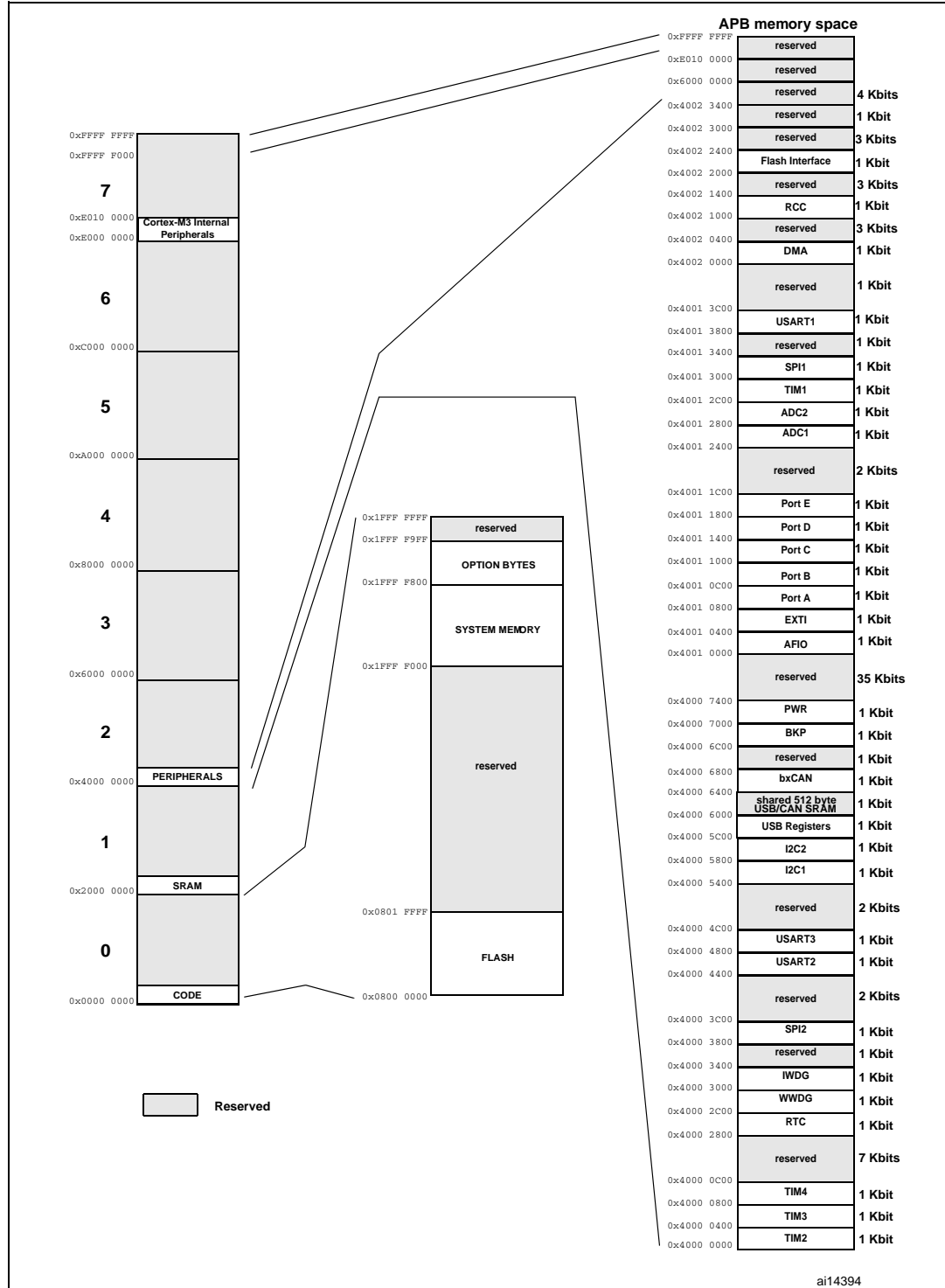
6. This alternate function can be remapped by software to some other port pins (if available on the used package). For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual, UM0306, available from the STMicroelectronics website: [www.st.com](http://www.st.com).

7. For the LQFP48 and LQFP64 packages, the pins number 5 and 6 are configured as OSC\_IN/OSC\_OUT after reset, however the functionality of PD0 and PD1 can be remapped by software on these pins.

# 4 Memory mapping

The memory map is shown in *Figure 6*.

Figure 6. Memory map



ai14394

## 5 Electrical characteristics

### 5.1 Test conditions

Unless otherwise specified, all voltages are referred to  $V_{SS}$ .

#### 5.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at  $T_A=25^\circ\text{C}$  and  $T_A=T_{A\text{max}}$  (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation ( $\text{mean}\pm 3\Sigma$ ).

#### 5.1.2 Typical values

Unless otherwise specified, typical data are based on  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3.3\text{ V}$  (for the  $2\text{ V} \leq V_{DD} \leq 3.6\text{ V}$  voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated ( $\text{mean}\pm 2\Sigma$ ).

#### 5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

#### 5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in [Figure 7](#).

#### 5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in [Figure 8](#).

Figure 7. Pin loading conditions

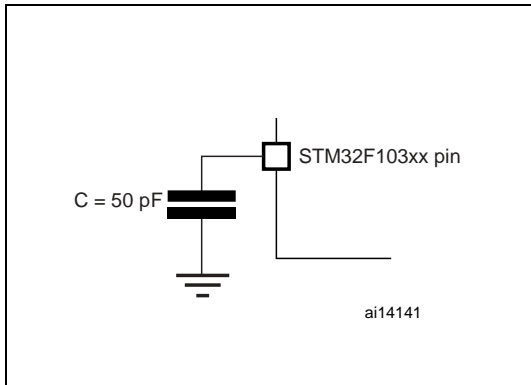
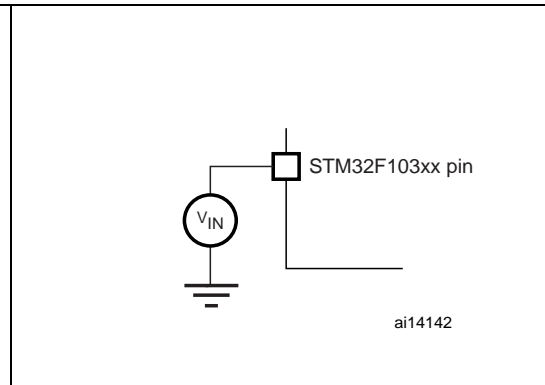
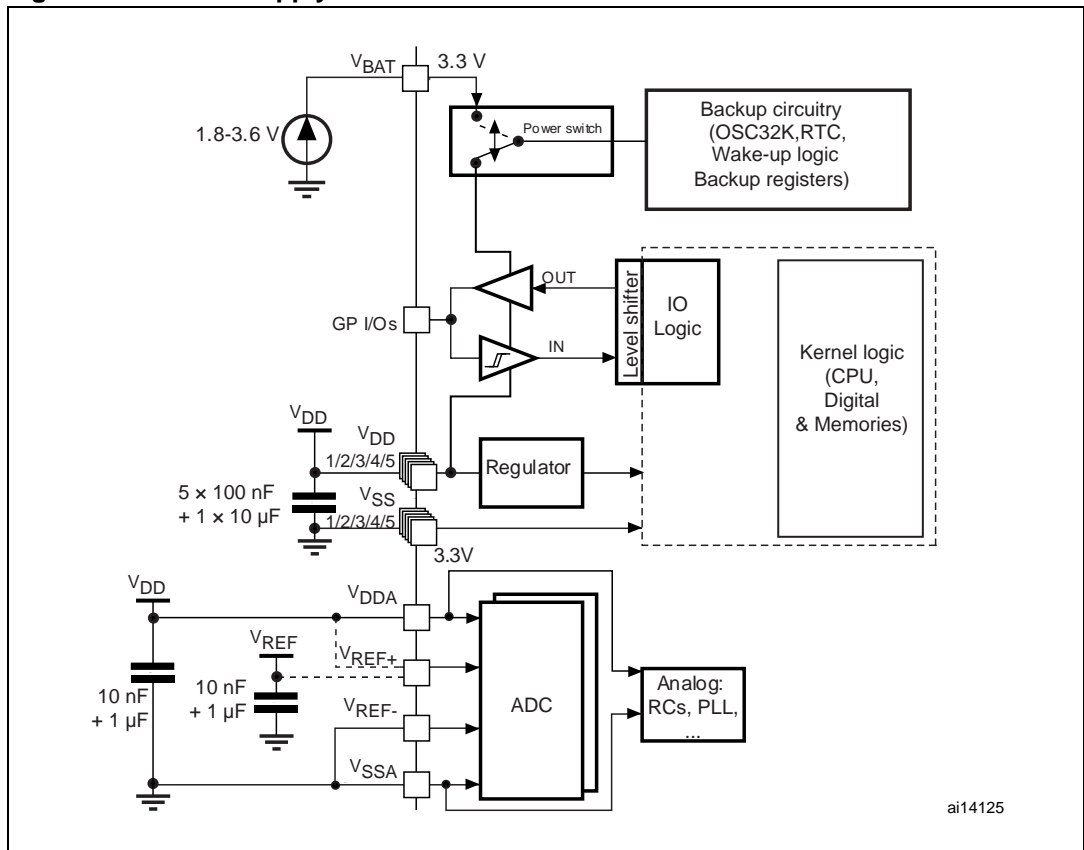


Figure 8. Pin input voltage



### 5.1.6 Power supply scheme

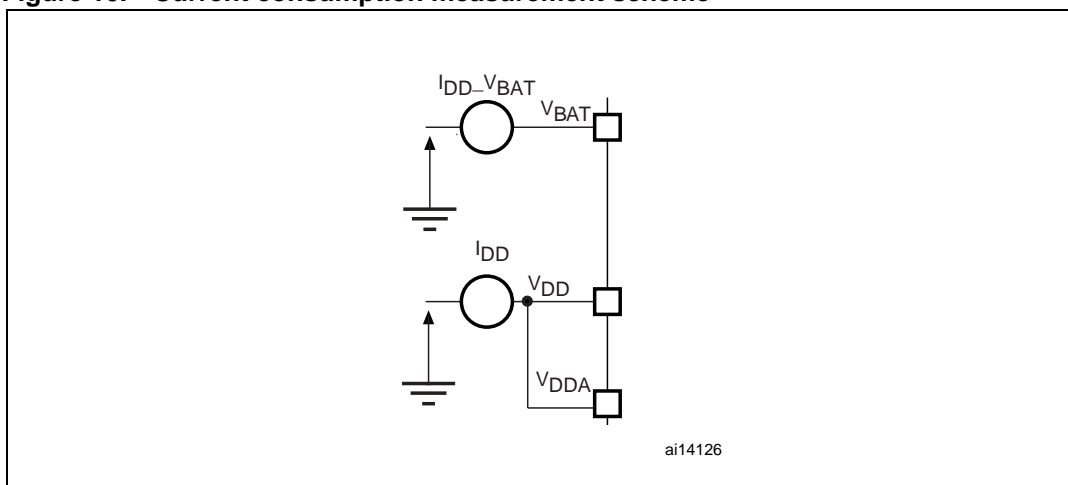
Figure 9. Power supply scheme





### 5.1.7 Current consumption measurement

Figure 10. Current consumption measurement scheme



## 5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in [Table 4: Voltage characteristics](#), [Table 5: Current characteristics](#), and [Table 6: Thermal characteristics](#) may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Table 4. Voltage characteristics**

Symbol	Ratings	Min	Max	Unit
$V_{DD}-V_{SS}$	External 3.3 V supply voltage (including $V_{DDA}$ and $V_{DD}$ ) <sup>(1)</sup>	-0.3	4.0	V
$V_{IN}$	Input voltage on five volt tolerant pin <sup>(2)</sup>	$V_{SS}-0.3$	+5.5	
	Input voltage on any other pin <sup>(2)</sup>	$V_{SS}-0.3$	$V_{DD}+0.3$	
$ \Delta V_{DDX} $	Variations between different power pins	50	50	mV
$ V_{SSX}-V_{SS} $	Variations between all the different ground pins	50	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see <a href="#">Section 5.3.11: Absolute maximum ratings (electrical sensitivity)</a>		

- All 3.3 V power ( $V_{DD}$ ,  $V_{DDA}$ ) and ground ( $V_{SS}$ ,  $V_{SSA}$ ) pins must always be connected to the external 3.3 V supply.
- $I_{INJ(PIN)}$  must never be exceeded (see [Table 5: Current characteristics](#)). This is implicitly insured if  $V_{IN}$  maximum is respected. If  $V_{IN}$  maximum cannot be respected, the injection current must be limited externally to the  $I_{INJ(PIN)}$  value. A positive injection is induced by  $V_{IN} > V_{DD}$  while a negative injection is induced by  $V_{IN} < V_{SS}$ .

**Table 5. Current characteristics**

Symbol	Ratings	Max.	Unit
$I_{VDD}$	Total current into $V_{DD}$ power lines (source) <sup>(1)</sup>	150	mA
$I_{VSS}$	Total current out of $V_{SS}$ ground lines (sink) <sup>(1)</sup>	150	
$I_{IO}$	Output current sunk by any I/O and control pin	25	
	Output current source by any I/Os and control pin	-25	
$I_{INJ(PIN)}$ <sup>(2)(3)</sup>	Injected current on NRST pin	± 5	
	Injected current on HSE OSC_IN and LSE OSC_IN pins	± 5	
	Injected current on any other pin <sup>(4)</sup>	± 5	
$\Sigma I_{INJ(PIN)}$ <sup>(2)</sup>	Total injected current (sum of all I/O and control pins) <sup>(4)</sup>	± 25	

- All 3.3 V power ( $V_{DD}$ ,  $V_{DDA}$ ) and ground ( $V_{SS}$ ,  $V_{SSA}$ ) pins must always be connected to the external 3.3 V supply.
- $I_{INJ(PIN)}$  must never be exceeded. This is implicitly insured if  $V_{IN}$  maximum is respected. If  $V_{IN}$  maximum cannot be respected, the injection current must be limited externally to the  $I_{INJ(PIN)}$  value. A positive injection is induced by  $V_{IN} > V_{DD}$  while a negative injection is induced by  $V_{IN} < V_{SS}$ .
- Negative injection disturbs the analog performance of the device. See note in [Section 5.3.17: 12-bit ADC characteristics](#).
- When several inputs are submitted to a current injection, the maximum  $\Sigma I_{INJ(PIN)}$  is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with  $\Sigma I_{INJ(PIN)}$  maximum current injection on four I/O port pins of the device.

**Table 6. Thermal characteristics**

Symbol	Ratings	Value	Unit
$T_{STG}$	Storage temperature range	-65 to +150	°C
$T_J$	Maximum junction temperature (see Thermal characteristics)		

## 5.3 Operating conditions

### 5.3.1 General operating conditions

**Table 7. General operating conditions**

Symbol	Parameter	Conditions	Min	Max	Unit
$f_{HCLK}$	Internal AHB clock frequency		0	72	MHz
$f_{PCLK1}$	Internal APB1 clock frequency		0	36	
$f_{PCLK2}$	Internal APB2 clock frequency		0	72	
$V_{DD}$	Standard operating voltage		2	3.6	V
$V_{BAT}$	Backup operating voltage		1.8	3.6	V
$T_A$	Ambient temperature range		-40	105	°C

### 5.3.2 Operating conditions at power-up / power-down

The parameters given in [Table 8](#) are derived from tests performed under the ambient temperature condition summarized in [Table 7](#).

**Table 8. Operating conditions at power-up / power-down**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{VDD}$	$V_{DD}$ rise/fall time rate		20			µs/V
					20	ms/V

### 5.3.3 Embedded reset and power control block characteristics

The parameters given in [Table 9](#) are derived from tests performed under ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 7](#).

**Table 9. Embedded reset and power control block characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{PVD}$	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)	2.1	2.18	2.26	V
		PLS[2:0]=000 (falling edge)	2	2.08	2.16	V
		PLS[2:0]=001 (rising edge)	2.19	2.28	2.37	V
		PLS[2:0]=001 (falling edge)	2.09	2.18	2.27	V
		PLS[2:0]=010 (rising edge)	2.28	2.38	2.48	V
		PLS[2:0]=010 (falling edge)	2.18	2.28	2.38	V
		PLS[2:0]=011 (rising edge)	2.38	2.48	2.58	V
		PLS[2:0]=011 (falling edge)	2.28	2.38	2.48	V
		PLS[2:0]=100 (rising edge)	2.47	2.58	2.69	V
		PLS[2:0]=100 (falling edge)	2.37	2.48	2.59	V
		PLS[2:0]=101 (rising edge)	2.57	2.68	2.79	V
		PLS[2:0]=101 (falling edge)	2.47	2.58	2.69	V
		PLS[2:0]=110 (rising edge)	2.66	2.78	2.9	V
		PLS[2:0]=110 (falling edge)	2.56	2.68	2.8	V
		PLS[2:0]=111 (rising edge)	2.76	2.88	3	V
		PLS[2:0]=111 (falling edge)	2.66	2.78	2.9	V
$V_{PVDhyst}$	PVD hysteresis			100		mV
$V_{POR/PDR}$	Power on/power down reset threshold	Falling edge	1.8	1.88	1.96	V
		Rising edge	1.84	1.92	2.0	V
$V_{PDRhyst}$	PDR hysteresis		40			mV
$T_{RSTTEMPO}$	Reset temporization		1	2.5	4.5	mS

### 5.3.4 Embedded reference voltage

The parameters given in [Table 10](#) are derived from tests performed under ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 7](#).

**Table 10. Embedded internal reference voltage**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{REFINT}$	Internal reference voltage	$-45^{\circ}\text{C} < T_A < +105^{\circ}\text{C}$	1.16	1.20	1.26	V
		$-45^{\circ}\text{C} < T_A < +85^{\circ}\text{C}$	1.16	1.20	1.24	V

### 5.3.5 Supply current characteristics

The current consumption is measured as described in [Figure 10: Current consumption measurement scheme](#).

#### Maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at  $V_{DD}$  or  $V_{SS}$  (no load)
- All peripherals are disabled except if it is explicitly mentioned
- The Flash access time is adjusted to  $f_{HCLK}$  frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above)

The parameters given in [Table 11](#) are derived from tests performed under ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 7](#).

**Table 11. Maximum current consumption in Run and Sleep modes<sup>(1)</sup>**

Symbol	Parameter	Conditions	$f_{HCLK}$	Typ <sup>(2)</sup>	Max <sup>(3)</sup>		Unit
					$T_A = 85\text{ }^\circ\text{C}$	$T_A = 105\text{ }^\circ\text{C}$	
$I_{DD}$	Supply current in Run mode	External clock with PLL, code running from Flash, all peripherals enabled (see RCC register description): $f_{PCLK1} = f_{HCLK}/2, f_{PCLK2} = f_{HCLK}$	72 MHz	36	TBD	TBD	mA
			48 MHz	30	TBD	TBD	
			36 MHz	22	TBD	TBD	
			24 MHz	21	TBD	TBD	
		External clock, PLL stopped, code running from Flash, all peripherals enabled (see RCC register description): $f_{PCLK1} = f_{HCLK}/2, f_{PCLK2} = f_{HCLK}$	8 MHz	10	TBD	TBD	
	Supply current in Sleep mode	External clock with PLL, code running from RAM, all peripherals enabled (see RCC register description): $f_{PCLK1} = f_{HCLK}/2, f_{PCLK2} = f_{HCLK}$	72 MHz	32	45	47	
			48 MHz	22	31	33	
			36 MHz	13	18	20	
			24 MHz	11	15	17	
		External clock, PLL stopped, code running from RAM, all peripherals enabled (see RCC register description): $f_{PCLK1} = f_{HCLK}/2, f_{PCLK2} = f_{HCLK}$	8 MHz	4.5	TBD	TBD	
Supply current in Sleep mode	External clock with PLL, code running from RAM or Flash, all peripherals enabled (see RCC register description): $f_{PCLK1} = f_{HCLK}/2, f_{PCLK2} = f_{HCLK}$	72 MHz	22	35	37	mA	
		48 MHz	14	23	25		
		36 MHz	13	22	24		
		24 MHz	10	17	19		
	External clock, PLL stopped, code running from RAM or Flash, all peripherals enabled (see RCC register description): $f_{PCLK1} = f_{HCLK}/2, f_{PCLK2} = f_{HCLK}$	8 MHz	3.5	TBD	TBD		

1. TBD stands for to be determined.
2. Typical values are measured at  $T_A = 25\text{ }^\circ\text{C}$ , and  $V_{DD} = 3.3\text{ V}$
3. Data based on characterization results, tested in production at  $V_{Dmax}, f_{HCLK} \text{ max. } T_{Amax}$ , and code executed from RAM.

**Table 12. Maximum current consumption in Stop and Standby modes<sup>(1)</sup>**

Symbol	Parameter	Conditions	Typ <sup>(2)</sup>		Max <sup>(3)</sup>		Unit
			V <sub>DD</sub> /V <sub>BAT</sub> = 2.4 V	V <sub>DD</sub> /V <sub>BAT</sub> = 3.3 V	T <sub>A</sub> = 85 °C	T <sub>A</sub> = 105 °C	
I <sub>DD</sub>	Supply current in Stop mode	Regulator in Run mode, Low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	TBD	24	TBD	TBD	µA
		Regulator in Low Power mode, Low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	TBD <sup>(4)</sup>	14 <sup>(4)</sup>	TBD <sup>(4)</sup>	TBD <sup>(4)</sup>	
	Supply current in Standby mode <sup>(5)</sup>	Low-speed internal RC oscillator and independent watchdog OFF, low-speed oscillator and RTC OFF	TBD <sup>(4)</sup>	2 <sup>(4)</sup>	TBD <sup>(4)</sup>	TBD <sup>(4)</sup>	
I <sub>DD_VBAT</sub>	Backup domain supply current	Low-speed oscillator and RTC ON	1 <sup>(4)</sup>	1.4 <sup>(4)</sup>	TBD <sup>(4)</sup>	TBD <sup>(4)</sup>	

1. TBD stands for to be determined.
2. Typical values are measured at T<sub>A</sub> = 25 °C, V<sub>DD</sub> = 3.3 V, unless otherwise specified.
3. Data based on characterization results, tested in production at V<sub>DD max</sub>, f<sub>HCLK max</sub>. and T<sub>A max</sub> (for other temperature).
4. Values expected for next silicon revision.
5. To have the Standby consumption with RTC ON, add I<sub>DD\_VBAT</sub> (Low-speed oscillator and RTC ON) to I<sub>DD Standby</sub> (when V<sub>DD</sub> is present the Backup Domain is powered by V<sub>DD</sub> supply).

**Typical current consumption**

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at  $V_{DD}$  or  $V_{SS}$  (no load).
- All peripherals are disabled except if it is explicitly mentioned.
- The Flash access time is adjusted to  $f_{HCLK}$  frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above).
- Ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 7](#).

**Table 13. Typical current consumption in Run and Sleep modes<sup>(1)</sup>**

Symbol	Parameter	Conditions	$f_{HCLK}$	Typ <sup>(2)</sup>	Unit
$I_{DD}$	Supply current in Run mode	Oscillator running at 8 MHz with PLL, code running from Flash, all peripheral disabled (see RCC register description): $f_{PCLK1} = f_{HCLK}/2$ , $f_{PCLK2} = f_{HCLK}$	72 MHz	21	mA
			48 MHz	18	
			36 MHz	TBD	
			24 MHz	13	
			16 MHz	TBD	
		Running on HSI clock, code running from Flash, all peripheral disabled (see RCC register description): $f_{PCLK1} = f_{HCLK}/2$ , $f_{PCLK2} = f_{HCLK}$ . AHB pre-scaler used to reduce the frequency	8 MHz	7.8	mA
			4 MHz	7	
			2 MHz	6.3	
			1 MHz	6.2	
			500 kHz	6.1	
	Running on HSI clock, code running from RAM, all peripheral disabled (see RCC register description): $f_{PCLK1} = f_{HCLK}/2$ , $f_{PCLK2} = f_{HCLK}$ . AHB pre-scaler used to reduce the frequency	8 MHz	2.3	mA	
		4 MHz	1.6		
		2 MHz	1.2		
		1 MHz	1		
		500 kHz	0.88		
Supply current in Sleep mode	Oscillator running at 8MHz with PLL, code running from Flash, all peripheral disabled (see RCC register description): $f_{PCLK1} = f_{HCLK}/2$ , $f_{PCLK2} = f_{HCLK}$	72 MHz	6	mA	
		48 MHz	TBD		
		36 MHz	TBD		
		24 MHz	TBD		
		16 MHz	1		
	Running on HSI clock, code running from Flash, all peripheral disabled (see RCC register description): $f_{PCLK1} = f_{HCLK}/2$ , $f_{PCLK2} = f_{HCLK}$ . AHB pre-scaler used to reduce the frequency	8 MHz	TBD	mA	
		4 MHz	TBD		
		2 MHz	TBD		
		1 MHz	TBD		
		500 kHz	TBD		

1. TBD stands for to be determined.  
 2. Typical values are measures at  $T_A = 25\text{ }^\circ\text{C}$ ,  $V_{DD} = 3.3\text{ V}$ .

**Table 14. Typical current consumption in Stop and Standby modes<sup>(1)</sup>**

Symbol	Parameter	Conditions	V <sub>DD</sub>	Typ <sup>(2)</sup>	Unit
I <sub>DD</sub>	Supply current in Stop mode	Regulator in Run mode, Low-speed and high-speed internal RC oscillators OFF High-speed oscillator OFF (no independent watchdog)	3.3 V	24	μA
			2.4 V	TBD	
		Regulator in Low Power mode, Low-speed and high-speed internal RC oscillators OFF, High-speed oscillator OFF (no independent watchdog)	3.3 V	14 <sup>(3)</sup>	
			2.4 V	TBD <sup>(3)</sup>	
	Supply current in Standby mode <sup>(4)</sup>	Low-speed internal RC oscillator and independent watchdog OFF	3.3 V	2 <sup>(3)</sup>	μA
			2.4 V	TBD <sup>(3)</sup>	
		Low-speed internal RC oscillator and independent watchdog ON	3.3 V	3.1 <sup>(3)</sup>	
			2.4 V	TBD <sup>(3)</sup>	
Low-speed internal RC oscillator ON, independent watchdog OFF		3.3 V	2.9 <sup>(3)</sup>		
		2.4 V	TBD <sup>(3)</sup>		
I <sub>DD_VBAT</sub>	Backup domain supply current	Low-speed oscillator and RTC ON	3.3 V	1.4 <sup>(3)</sup>	μA
			2.4 V	1 <sup>(3)</sup>	
		Low-speed oscillator OFF, RTC ON	3.3 V	0.5 <sup>(3)</sup>	
			2.4 V	TBD <sup>(3)</sup>	

1. TBD stands for to be determined.
2. Typical values are measures at T<sub>A</sub> = 25 °C, V<sub>DD</sub> = 3.3 V.
3. Values expected for next silicon revision.
4. To obtain Standby consumption with RTC ON, add I<sub>DD\_VBAT</sub> (Low-speed oscillator and RTC ON) to I<sub>DD</sub> Standby.



### 5.3.6 External clock source characteristics

#### High-speed external user clock

The characteristics given in [Table 15](#) result from tests performed using an high-speed external clock source, and under ambient temperature and supply voltage conditions summarized in [Table 7](#).

**Table 15. High-speed external (HSE) user clock characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{\text{HSE\_ext}}$	User external clock source frequency <sup>(1)</sup>			8	25	MHz
$V_{\text{HSEH}}$	OSC_IN input pin high level voltage		$0.7V_{\text{DD}}$		$V_{\text{DD}}$	V
$V_{\text{HSEL}}$	OSC_IN input pin low level voltage		$V_{\text{SS}}$		$0.3V_{\text{DD}}$	
$t_{\text{w}}(\text{HSE})$ $t_{\text{w}}(\text{HSE})$	OSC_IN high or low time <sup>(1)</sup>		16			ns
$t_{\text{r}}(\text{HSE})$ $t_{\text{f}}(\text{HSE})$	OSC_IN rise or fall time <sup>(1)</sup>				5	
$I_{\text{L}}$	OSC_IN Input leakage current	$V_{\text{SS}} \leq V_{\text{IN}} \leq V_{\text{DD}}$			$\pm 1$	$\mu\text{A}$

1. Value based on design simulation and/or technology characteristics. It is not tested in production.

#### Low-speed external user clock

The characteristics given in [Table 16](#) result from tests performed using an low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in [Table 7](#).

**Table 16. Low-speed external user clock characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{\text{LSE\_ext}}$	User External clock source frequency <sup>(1)</sup>			32.768	1000	kHz
$V_{\text{LSEH}}$	OSC32_IN input pin high level voltage		$0.7V_{\text{DD}}$		$V_{\text{DD}}$	V
$V_{\text{LSEL}}$	OSC32_IN input pin low level voltage		$V_{\text{SS}}$		$0.3V_{\text{DD}}$	
$t_{\text{w}}(\text{LSE})$ $t_{\text{w}}(\text{LSE})$	OSC32_IN high or low time <sup>(1)</sup>		450			ns
$t_{\text{r}}(\text{LSE})$ $t_{\text{f}}(\text{LSE})$	OSC32_IN rise or fall time <sup>(1)</sup>				5	
$I_{\text{L}}$	OSC32_IN Input leakage current	$V_{\text{SS}} \leq V_{\text{IN}} \leq V_{\text{DD}}$			$\pm 1$	$\mu\text{A}$

1. Value based on design simulation and/or technology characteristics. It is not tested in production.

Figure 11. High-speed external clock source AC timing diagram

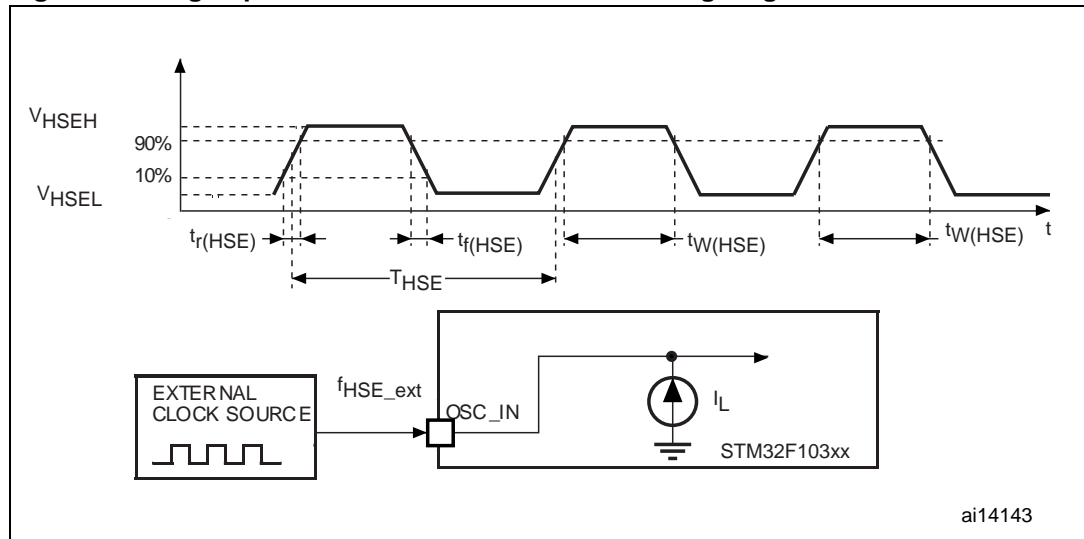
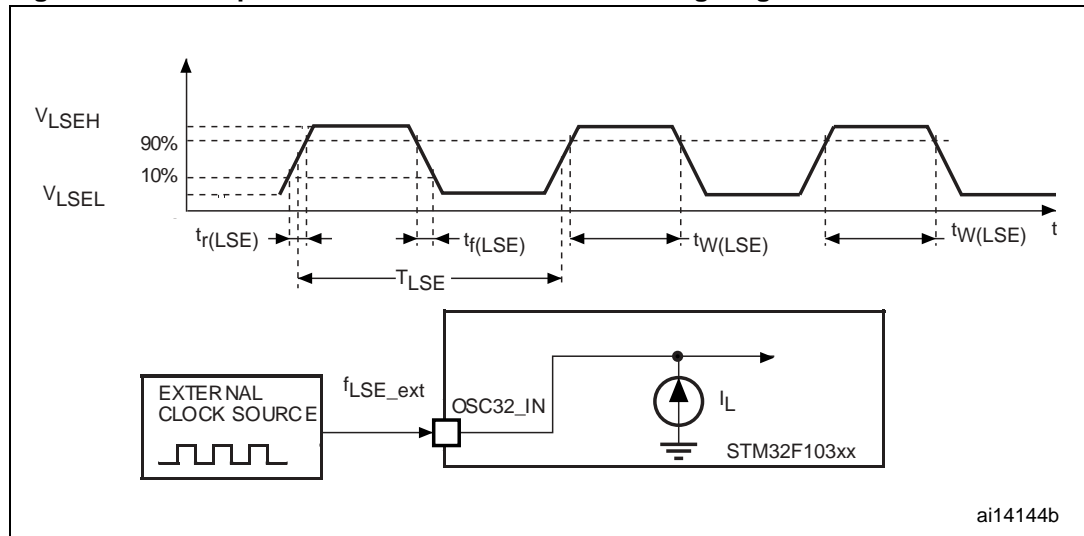


Figure 12. Low-speed external clock source AC timing diagram



### High-speed external clock

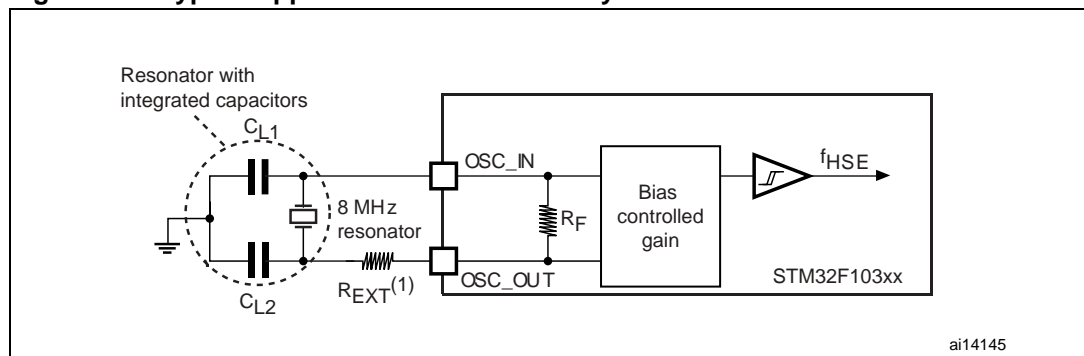
The high-speed external (HSE) clock can be supplied with a 4 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in [Table 17](#). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

**Table 17. HSE 4-16 MHz oscillator characteristics<sup>(1)</sup>**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{OSC\_IN}$	Oscillator frequency		4	8	16	MHz
$R_F$	Feedback resistor			200		k $\Omega$
$C_{L1}$ $C_{L2}$ <sup>(2)</sup>	Recommended load capacitance versus equivalent serial resistance of the crystal ( $R_S$ ) <sup>(3)</sup>	$R_S = 30 \Omega$		30		pF
$i_2$	HSE driving current	$V_{DD} = 3.3 V$ $V_{IN} = V_{SS}$ with 30 pF load			1	mA
$g_m$	Oscillator Transconductance	Startup	25			mA/V
$t_{SU(HSE)}$ <sup>(4)</sup>	startup time	$V_{SS}$ is stabilized		2		ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. For  $C_{L1}$  and  $C_{L2}$  it is recommended to use high-quality ceramic capacitors in the 5 pF to 25pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator.  $C_{L1}$  and  $C_{L2}$  are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of  $C_{L1}$  and  $C_{L2}$ . PCB and MCU pin capacitance must be included when sizing  $C_{L1}$  and  $C_{L2}$  (10 pF can be used as a rough estimate of the combined pin and board capacitance).
3. The relatively low value of the  $R_F$  resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
4.  $t_{SU(HSE)}$  is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

**Figure 13. Typical application with a 8-MHz crystal**



1.  $R_{EXT}$  value depends on the crystal characteristics. Typical value is in the range of 5 to 6 $R_S$ .

**Low-speed external clock**

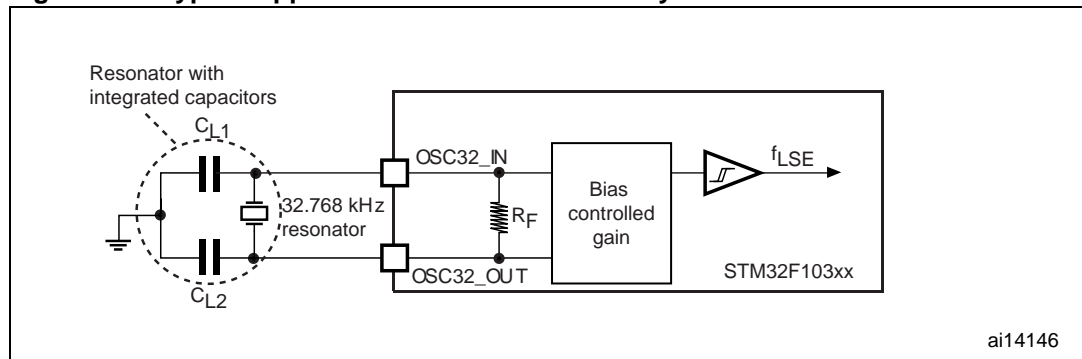
The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in [Table 18](#). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

**Table 18. LSE oscillator characteristics ( $f_{LSE} = 32.768$  kHz)**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_F$	Feedback resistor			5		$M\Omega$
$C_{L1}$ $C_{L2}$	Recommended load capacitance versus equivalent serial resistance of the crystal ( $R_S$ ) <sup>(1)</sup>	$R_S = 30$ k $\Omega$			15	pF
$I_2$	LSE driving current	$V_{DD} = 3.3$ V $V_{IN} = V_{SS}$			1.4	$\mu$ A
$g_m$	Oscillator Transconductance		5			$\mu$ A/V
$t_{SU(LSE)}$ <sup>(2)</sup>	startup time	$V_{SS}$ is stabilized		3		s

1. The oscillator selection can be optimized in terms of supply current using an high quality resonator with small  $R_S$  value for example MSIV-TIN32.768kHz. Refer to crystal manufacturer for more details
2.  $t_{SU(LSE)}$  is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

**Figure 14. Typical application with a 32.768 kHz crystal**



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### 5.3.7 Internal clock source characteristics

The parameters given in [Table 19](#) are derived from tests performed under ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 7](#).

#### High-speed internal (HSI) RC oscillator

**Table 19. HSI oscillator characteristics<sup>(1)(2)</sup>**

Symbol	Parameter	Conditions	Min	Typ	Max <sup>(3)</sup>	Unit
$f_{HSI}$	Frequency			8		MHz
$ACC_{HSI}$	Accuracy of HSI oscillator	$T_A = -40$ to $105$ °C	TBD	$\pm 3$	TBD	%
		at $T_A = 25$ °C	TBD	$\pm 1$	TBD	%
$t_{su(HSI)}$	HSI oscillator start up time		1		2	$\mu s$
$I_{DD(HSI)}$	HSI oscillator power consumption			80	100	$\mu A$

- $V_{DD} = 3.3$  V,  $T_A = -40$  to  $105$  °C unless otherwise specified.
- TBD stands for to be determined.
- Values based on device characterization, not tested in production.

#### LSI Low Speed Internal RC Oscillator

**Table 20. LSI oscillator characteristics<sup>(1)</sup>**

Symbol	Parameter	Conditions	Min	Typ	Max <sup>(2)</sup>	Unit
$f_{LSI}$	Frequency		30		60	kHz
$t_{su(LSI)}$	LSI oscillator start up time				85	$\mu s$
$I_{DD(LSI)}$	LSI oscillator power consumption			0.65	1.2	$\mu A$

- $V_{DD} = 3$  V,  $T_A = -40$  to  $105$  °C unless otherwise specified.
- Value based on device characterization, not tested in production.

### Wakeup time from low power mode

The wakeup times given in [Table 21](#) is measured on a wakeup phase with a 8-MHz HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

- Stop or Standby mode: the clock source is the RC oscillator
- Sleep mode: the clock source is the clock that was set before entering Sleep mode.

All timings are derived from tests performed under ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 7](#).

**Table 21. Low-power mode wakeup timings<sup>(1)</sup>**

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WUSLEEP}^{(2)}$	Wakeup from Sleep mode	Wakeup on HSI RC clock	0.75	TBD	$\mu s$
$t_{WUSTOP}^{(2)}$	Wakeup from Stop mode (regulator in run mode)	HSI RC wakeup time = 2 $\mu s$	4	TBD	$\mu s$
	Wakeup from Stop mode (regulator in low power mode)	HSI RC wakeup time = 2 $\mu s$ , Regulator wakeup from LP mode time = 5 $\mu s$	7	TBD	
$t_{WUSTDBY}^{(3)}$	Wakeup from Standby mode	HSI RC wakeup time = 2 $\mu s$ , Regulator wakeup from power down time = 38 $\mu s$	40	TBD	$\mu s$

1. TBD stands for to be determined.
2. The wakeup time from Sleep and Stop mode are measured from the wakeup event to the point in which the user application code reads the first instruction.
3. The wakeup time from Standby mode is measured from the wakeup event to the point in which the device exits from reset.

### 5.3.8 PLL characteristics

The parameters given in [Table 22](#) are derived from tests performed under ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 7](#).

**Table 22. PLL characteristics<sup>(1)</sup>**

Symbol	Parameter	Test Conditions	Value			Unit
			Min	Typ	Max <sup>(2)</sup>	
$f_{PLL\_IN}$	PLL input clock			8.0		MHz
	PLL input clock duty cycle		40		60	%
$f_{PLL\_OUT}$	PLL multiplier output clock		16		72	MHz
$f_{VCO}$	VCO frequency range	When PLL operates (locked)	32		144	MHz
$t_{LOCK}$	PLL lock time				200	$\mu s$
$t_{JITTER}$	Cycle to cycle jitter (+/-3 $\Sigma$ peak to peak)	$V_{DD}$ is stable	TBD		TBD	%

1. TBD stands for to be determined.
2. Data based on device characterization, not tested in production.

### 5.3.9 Memory characteristics

#### Flash memory

The characteristics are given at  $T_A = -40$  to  $+105$  °C unless otherwise specified.

**Table 23. Flash memory characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max <sup>(1)</sup>	Unit
$t_{prog}$	Word programming time	$T_A = -40$ to $+105$ °C	20		40	$\mu s$
$t_{ERASE}$	Page (1kB) erase time	$T_A = -40$ to $+105$ °C	20		40	ms
$t_{ME}$	Mass erase time	$T_A = -40$ to $+105$ °C	20		40	ms
$I_{DD}$	Supply current	Read mode $f_{HCLK} = 72$ MHz with 2 wait states, $V_{DD} = 3.3$ V			20	mA
		Write / Erase modes $f_{HCLK} = 72$ MHz, $V_{DD} = 3.3$ V			5	mA
		Power-down mode / HALT, $V_{DD} = 3.0$ to $3.6$ V			50	$\mu A$

1. Values based on characterization and not tested in production.

**Table 24. Flash memory endurance and data retention**

Symbol	Parameter	Conditions	Value			Unit
			Min <sup>(1)</sup>	Typ	Max	
$N_{END}$	Endurance		1	10		kcycles
$t_{RET}$	Data retention	$T_A = 85$ °C	30			Years

1. Values based on characterization not tested in production.

### 5.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

#### Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 1000-4-2 standard.
- **FTB: A Burst of Fast Transient voltage** (positive and negative) is applied to  $V_{DD}$  and  $V_{SS}$  through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in [Table 25](#). They are based on the EMS levels and classes defined in application note AN1709.

**Table 25. EMS characteristics<sup>(1)</sup>**

Symbol	Parameter	Conditions	Level/Class
$V_{FESD}$	Voltage limits to be applied on any I/O pin to induce a functional disturbance	$V_{DD} = 3.3\text{ V}$ , $T_A = +25\text{ °C}$ , $f_{HCLK} = 48\text{ MHz}$ conforms to IEC 1000-4-2	TBD
$V_{EFTB}$	Fast transient voltage burst limits to be applied through 100pF on $V_{DD}$ and $V_{SS}$ pins to induce a functional disturbance	$V_{DD} = 3.3\text{ V}$ , $T_A = +25\text{ °C}$ , $f_{HCLK} = 48\text{ MHz}$ conforms to IEC 1000-4-4	4A

1. TBD stands for to be determined.

#### Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

#### Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)



### Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

### Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with SAE J 1752/3 standard which specifies the test board and the pin loading.

**Table 26. EMI characteristics**

Symbol	Parameter	Conditions	Monitored Frequency Band	Max vs. [f <sub>HSE</sub> /f <sub>HCLK</sub> ]		Unit
				8/48 MHz	8/72 MHz	
S <sub>EMI</sub>	Peak level	V <sub>DD</sub> = 3.3 V, T <sub>A</sub> = 25 °C, LQFP100 package compliant with SAE J 1752/3	0.1 to 30 MHz	12	12	dBμV
			30 to 130 MHz	22	19	
			130 MHz to 1GHz	23	29	
			SAE EMI Level	4	4	-

### 5.3.11 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

#### Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size is either 3 parts (cumulative mode) or 3 parts × (n + 1) supply pins (non-cumulative mode). The human body model (HBM) can be simulated. The tests are compliant with JESD22-A114A standard.

For more details, refer to the application note AN1181.

**Table 27. ESD absolute maximum ratings<sup>(1)</sup>**

Symbol	Ratings	Conditions	Maximum value <sup>(2)</sup>	Unit
V <sub>ESD(HBM)</sub>	Electrostatic discharge voltage (human body model)	T <sub>A</sub> = +25 °C	2000	V
V <sub>ESD(CDM)</sub>	Electrostatic discharge voltage (charge device model)		TBD	

1. TBD stands for to be determined.
2. Values based on characterization results, not tested in production.

#### Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

**Table 28. Electrical sensitivities**

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T <sub>A</sub> = +105 °C	II level A

### 5.3.12 I/O port pin characteristics

#### General input/output characteristics

Unless otherwise specified, the parameters given in [Table 29](#) are derived from tests performed under ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 7](#).

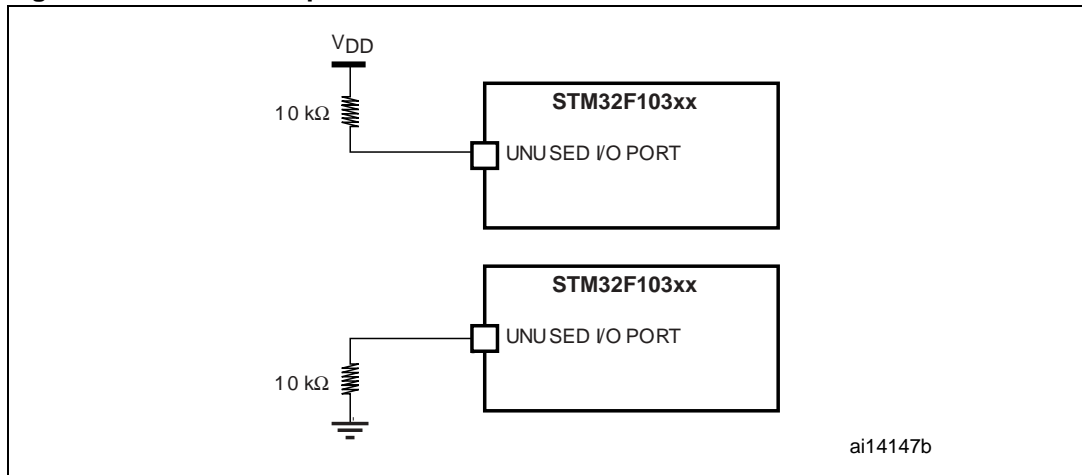
All unused pins must be held at a fixed voltage, by using the I/O output mode, an external pull-up or pull-down resistor (see [Figure 15](#)).

**Table 29. I/O static characteristics<sup>(1)</sup>**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL}$	Input low level voltage <sup>(2)</sup>	TTL ports	-0.5		0.8	V
$V_{IH}$	IO TC input high level voltage <sup>(2)</sup>		2		$V_{DD}+0.5$	
	IO FT high level voltage <sup>(2)</sup>		2		5.5V	
$V_{IL}$	Input low level voltage <sup>(2)</sup>	CMOS ports	-0.5		$0.35 V_{DD}$	V
$V_{IH}$	Input high level voltage <sup>(2)</sup>		$0.65 V_{DD}$		$V_{DD}+0.5$	
$V_{hys}$	IO TC Schmitt trigger voltage hysteresis <sup>(3)</sup>			200		mV
	IO TC Schmitt trigger voltage hysteresis <sup>(3)</sup>			$5\% V_{DD}$ <sup>(4)</sup>		mV
$I_{lkg}$	Input leakage current <sup>(5)</sup>	$V_{SS} \leq V_{IN} \leq V_{DD}$ Standard I/Os			$\pm 1$	$\mu A$
		$V_{IN} = 5 V$ 5 V tolerant I/Os			3	
$R_{PU}$	Weak pull-up equivalent resistor <sup>(6)</sup>	$V_{IN} = V_{SS}$	30	40	50	k $\Omega$
$R_{PD}$	Weak pull-down equivalent resistor <sup>(6)</sup>	$V_{IN} = V_{DD}$	30	40	50	k $\Omega$
$C_{IO}$	I/O pin capacitance			5		pF

- $V_{DD} = 3.3 V$ ,  $T_A = -40$  to  $105$  °C unless otherwise specified.
- Values based on characterization results, and not tested in production.
- Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested.
- With a minimum of 100 mV.
- Leakage could be higher than max. if negative current is injected on adjacent pins.
- Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This MOS/NMOS contribution to the series resistance is minimum (~10% order).

Figure 15. Unused I/O pin connection



### Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to +/-8 mA, and sink +20 mA (with a relaxed  $V_{OL}$ ).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in [Section 5.2](#):

- The sum of the currents sourced by all the I/Os on  $V_{DD}$ , plus the maximum Run consumption of the MCU sourced on  $V_{DD}$ , cannot exceed the absolute maximum rating  $I_{VDD}$  (see [Table 5](#)).
- The sum of the currents sunk by all the I/Os on  $V_{SS}$  plus the maximum Run consumption of the MCU sunk on  $V_{SS}$  cannot exceed the absolute maximum rating  $I_{VSS}$  (see [Table 5](#)).

### Output voltage levels

Unless otherwise specified, the parameters given in [Table 30](#) are derived from tests performed under ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 7](#).

**Table 30. Output voltage characteristics**

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin when 8 pins are sunk at same time	TTL port $I_{IO} = +8 \text{ mA}$ $2.7 \text{ V} < V_{DD} < 3.6 \text{ V}$		0.4	V
$V_{OH}^{(2)}$	Output high level voltage for an I/O pin when 4 pins are sourced at same time		$V_{DD}-0.4$		
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin when 8 pins are sunk at same time	CMOS port $I_{IO} = +8 \text{ mA}$ $2.7 \text{ V} < V_{DD} < 3.6 \text{ V}$		0.4	V
$V_{OH}^{(2)}$	Output high level voltage for an I/O pin when 4 pins are sourced at same time		2.4		
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin when 8 pins are sunk at same time	$I_{IO} = +20 \text{ mA}$ $2.7 \text{ V} < V_{DD} < 3.6 \text{ V}$		1.3	V
$V_{OH}^{(2)}$	Output high level voltage for an I/O pin when 4 pins are sourced at same time		$V_{DD}-1.3$		
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin when 8 pins are sunk at same time	$I_{IO} = +6 \text{ mA}$ $2 \text{ V} < V_{DD} < 2.7 \text{ V}$		0.4	V
$V_{OH}^{(2)}$	Output high level voltage for an I/O pin when 4 pins are sourced at same time		$V_{DD}-0.4$		

1. The  $I_{IO}$  current sunk by the device must always respect the absolute maximum rating specified in [Table 5](#) and the sum of  $I_{IO}$  (I/O ports and control pins) must not exceed  $I_{VSS}$ .
2. The  $I_{IO}$  current sourced by the device must always respect the absolute maximum rating specified in [Table 5](#) and the sum of  $I_{IO}$  (I/O ports and control pins) must not exceed  $I_{VDD}$ .

**Input/output AC characteristics**

The definition and values of input/output AC characteristics are given in [Figure 16](#) and [Table 31](#), respectively.

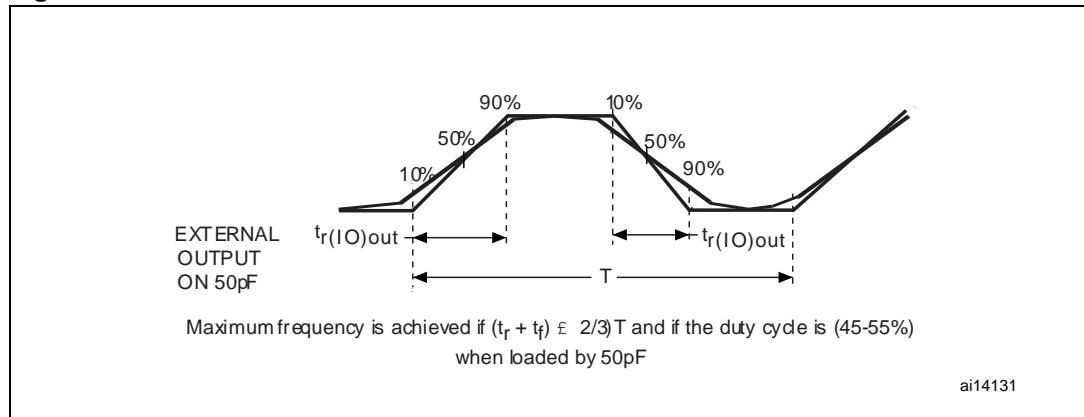
Unless otherwise specified, the parameters given in [Table 31](#) are derived from tests performed under ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 7](#).

**Table 31. I/O AC characteristics<sup>(1)</sup>**

I/O mode <sup>(1)</sup>	Symbol	Parameter	Conditions	Min	Max	Unit
10	$f_{max(IO)out}$	Maximum frequency <sup>(2)</sup>	$C_L = 50 \text{ pF}, V_{DD} = 2 \text{ V to } 3.6 \text{ V}$		2	MHz
	$t_{f(IO)out}$	Output high to low level fall time <sup>(3)</sup>	$C_L = 50 \text{ pF}, V_{DD} = 2 \text{ V to } 3.6 \text{ V}$		125	ns
	$t_{r(IO)out}$	Output low to high level rise time <sup>(3)</sup>			125	
01	$f_{max(IO)out}$	Maximum frequency <sup>(2)</sup>	$C_L = 50 \text{ pF}, V_{DD} = 2 \text{ V to } 3.6 \text{ V}$		10	MHz
	$t_{f(IO)out}$	Output high to low level fall time <sup>(3)</sup>	$C_L = 50 \text{ pF}, V_{DD} = 2 \text{ V to } 3.6 \text{ V}$		25	ns
	$t_{r(IO)out}$	Output low to high level rise time <sup>(3)</sup>			25	
11	$F_{max(IO)out}$	Maximum frequency <sup>(2)</sup>	$C_L = 30 \text{ pF}, V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$		50	MHz
			$C_L = 50 \text{ pF}, V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$		30	MHz
			$C_L = 50 \text{ pF}, V_{DD} = 2 \text{ V to } 2.7 \text{ V}$		20	MHz
	$t_{f(IO)out}$	Output high to low level fall time <sup>(3)</sup>	$C_L = 30 \text{ pF}, V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$		5	ns
			$C_L = 50 \text{ pF}, V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$		8	
			$C_L = 50 \text{ pF}, V_{DD} = 2 \text{ V to } 2.7 \text{ V}$		12	
	$t_{r(IO)out}$	Output low to high level rise time <sup>(3)</sup>	$C_L = 30 \text{ pF}, V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$		5	
			$C_L = 50 \text{ pF}, V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$		8	
			$C_L = 50 \text{ pF}, V_{DD} = 2 \text{ V to } 2.7 \text{ V}$		12	
-	$t_{EXTIpw}$	Pulse width of external signals detected by the EXTI controller		10		ns

1. Refer to the Reference user manual UM0306 for a description of GPIO Port configuration register.
2. The maximum frequency is defined in [Figure 16](#).
3. Values based on design simulation and validated on silicon, not tested in production.

Figure 16. I/O AC characteristics definition



### 5.3.13 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor,  $R_{PU}$  (see [Table 29](#)).

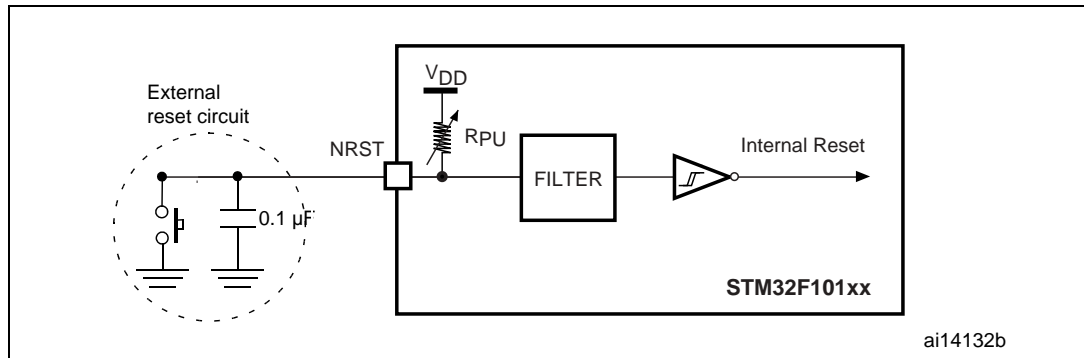
Unless otherwise specified, the parameters given in [Table 32](#) are derived from tests performed under ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 7](#).

Table 32. NRST pin characteristics<sup>(1)</sup>

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST Input low level voltage		-0.5		0.8	V
$V_{IH(NRST)}$	NRST Input high level voltage		2		$V_{DD}+0.5$	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis			200		
$R_{PU}$	Weak pull-up equivalent resistor <sup>(2)</sup>	$V_{IN} = V_{SS}$	30	40	50	$k\Omega$
$V_{F(NRST)}$	NRST Input filtered pulse <sup>(3)</sup>				100	ns
$V_{NF(NRST)}$	NRST Input not filtered pulse <sup>(3)</sup>		300			$\mu s$

1. TBD stands for to be determined.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).
3. Values guaranteed by design, not tested in production.

Figure 17. Recommended NRST pin protection



2. The reset network protects the device against parasitic resets.
3. The user must ensure that the level on the NRST pin can go below the  $V_{IL(NRST)}$  max level specified in [Table 32](#). Otherwise the reset will not be taken into account by the device.

### 5.3.14 TIM timer characteristics

Unless otherwise specified, the parameters given in [Table 33](#) are derived from tests performed under ambient temperature,  $f_{PCLKx}$  frequency and  $V_{DD}$  supply voltage conditions summarized in [Table 7](#).

Refer to [Section 5.3.12: I/O port pin characteristics](#) for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 33. TIMx<sup>(1)</sup> characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time		1		$t_{TIMxCLK}$
		$f_{TIMxCLK} = 72 \text{ MHz}$	13.9		ns
$f_{EXT}$	Timer external clock frequency on CH1 to CH4		0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK} = 72 \text{ MHz}$	0	36	MHz
$Res_{TIM}$	Timer resolution			16	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected		1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 72 \text{ MHz}$	0.0139	910	µs
$t_{MAX\_COUNT}$	Maximum possible count			$65536 \times 65536$	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 72 \text{ MHz}$		59.6	s

1. TIMx is used as a general term to refer to the TIM1, TIM2, TIM3 and TIM4 timers.



### 5.3.15 Communications interfaces

#### I<sup>2</sup>C interface characteristics

Unless otherwise specified, the parameters given in [Table 34](#) are derived from tests performed under ambient temperature,  $f_{PCLK1}$  frequency and  $V_{DD}$  supply voltage conditions summarized in [Table 7](#).

The STM32F103xx performance line I<sup>2</sup>C interface meets the requirements of the standard I<sup>2</sup>C communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and  $V_{DD}$  is disabled, but is still present. In addition, there is a protection diode between the I/O pin and  $V_{DD}$ . As a consequence, when multiple master devices are connected to the I<sup>2</sup>C bus, it is not possible to power off the STM32F103xx while another I<sup>2</sup>C master node remains powered on. Otherwise, the STM32F103xx would be powered by the protection diode.

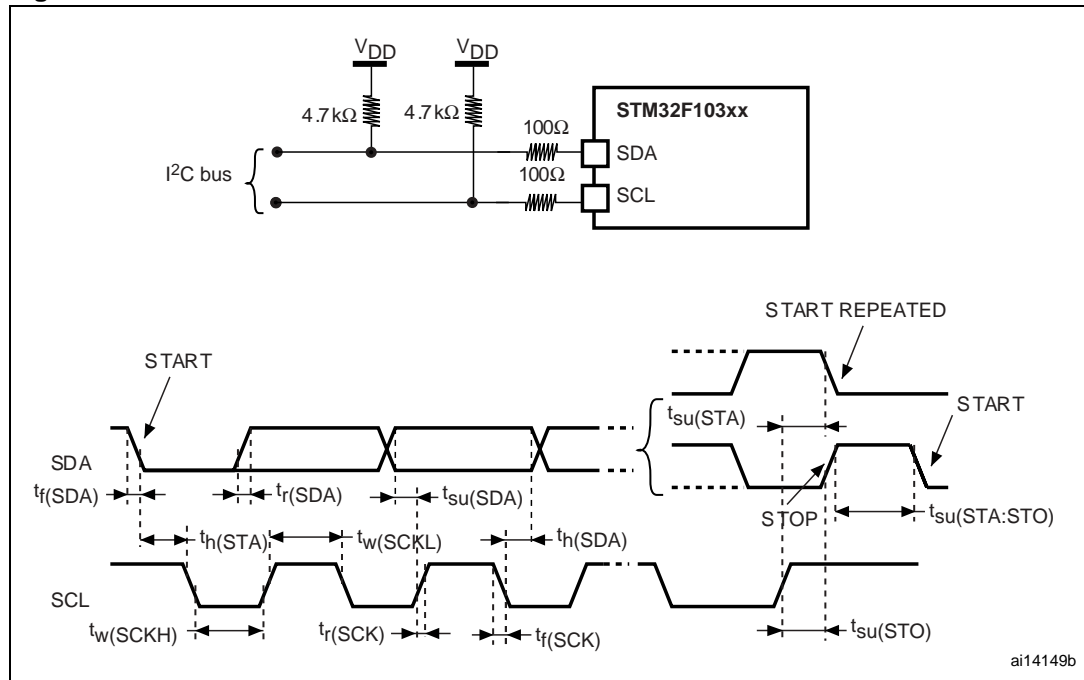
The I<sup>2</sup>C characteristics are described in [Table 34](#). Refer also to [Section 5.3.12: I/O port pin characteristics](#) for more details on the input/output alternate function characteristics (SDA and SCL).

**Table 34. I<sup>2</sup>C characteristics**

Symbol	Parameter	Standard mode I <sup>2</sup> C <sup>(1)</sup>		Fast mode I <sup>2</sup> C <sup>(1)(2)</sup>		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		$\mu$ s
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_h(SDA)$	SDA data hold time	0 <sup>(3)</sup>		0 <sup>(4)</sup>	900 <sup>(3)</sup>	
$t_r(SDA)$ $t_r(SCL)$	SDA and SCL rise time		1000	$20 + 0.1C_b$	300	
$t_f(SDA)$ $t_f(SCL)$	SDA and SCL fall time		300	$20 + 0.1C_b$	300	
$t_h(STA)$	Start condition hold time	4.0		0.6		$\mu$ s
$t_{su(STA)}$	Repeated Start condition setup time	4.7		0.6		
$t_{su(STO)}$	Stop condition setup time	4.0		0.6		$\mu$ s
$t_w(STO:STA)$	Stop to Start condition time (bus free)	4.7		1.3		$\mu$ s
$C_b$	Capacitive load for each bus line		400		400	pF

1. Values based on standard I<sup>2</sup>C protocol requirement, not tested in production.
2.  $f_{PCLK1}$  must be higher than 2 MHz to achieve the maximum standard mode I<sup>2</sup>C frequency. It must be higher than 4 MHz to achieve the maximum fast mode I<sup>2</sup>C frequency.
3. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.
4. The device must internally provide a hold time of at least 300ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.

Figure 18. I<sup>2</sup>C bus AC waveforms and measurement circuit



1. Measurement points are done at CMOS levels: 0.3V<sub>DD</sub> and 0.7V<sub>DD</sub>.

Table 35. SCL frequency (f<sub>PCLK1</sub> = 36 MHz, V<sub>DD</sub> = 3.3 V)<sup>(1)(2)(3)</sup>

f <sub>SCL</sub> (kHz)	I2C_CCR value
	R <sub>P</sub> = 4.7 kΩ
400	TBD
300	TBD
200	TBD
100	TBD
50	TBD
20	TBD

1. TBD = to be determined.
2. R<sub>P</sub> = External pull-up resistance, f<sub>SCL</sub> = I<sup>2</sup>C speed,
3. For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed is ±2%. These variations depend on the accuracy of the external components used to design the application.

### SPI interface characteristics

Unless otherwise specified, the parameters given in [Table 36](#) are derived from tests performed under ambient temperature,  $f_{PCLKx}$  frequency and  $V_{DD}$  supply voltage conditions summarized in [Table 7](#).

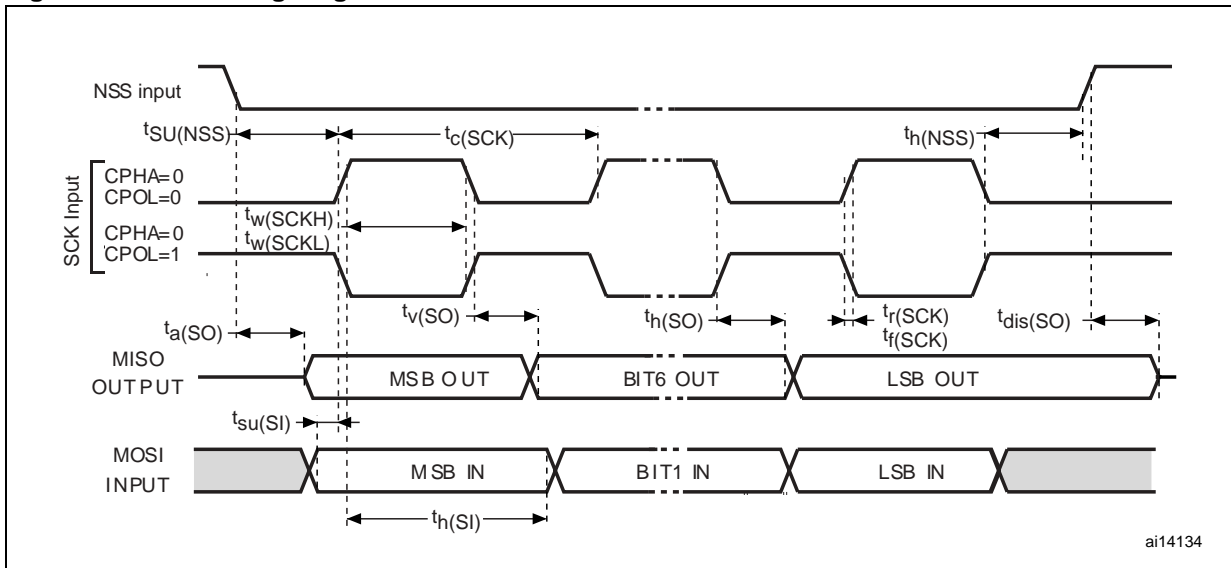
Refer to [Section 5.3.12: I/O port pin characteristics](#) for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

**Table 36. SPI characteristics<sup>(1)</sup>**

Symbol	Parameter	Conditions	Min	Max	Unit
$f_{SCK}$ $1/t_{c(SCK)}$	SPI clock frequency	Master mode	TBD	TBD	MHz
		Slave mode	0	TBD	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C=50 pF		TBD	ns
$t_{su(NSS)}^{(2)}$	NSS setup time	Slave mode	0		
$t_{h(NSS)}^{(2)}$	NSS hold time	Slave mode	0		
$t_{w(SCKH)}^{(2)}$ $t_{w(SCKL)}^{(2)}$	SCK high and low time	Master mode, $f_{PCLK} = \text{TBD}$ , presc = TBD	TBD		
$t_{su(MI)}^{(2)}$ $t_{su(SI)}^{(2)}$	Data input setup time	Master mode	TBD		
		Slave mode	TBD		
$t_{h(MI)}^{(2)}$ $t_{h(SI)}^{(2)}$	Data input hold time	Master mode	TBD		
		Slave mode	TBD		
		Master mode, $f_{PCLK} = \text{TBD}$	TBD <sup>(3)</sup>		
		Slave mode, $f_{PCLK} = \text{TBD}$	TBD <sup>(3)</sup>		
$t_{a(SO)}^{(2)(4)}$	Data output access time	Slave mode	TBD	TBD	
		Slave mode, $f_{PCLK} = \text{TBD}$	TBD	TBD	
$t_{dis(SO)}^{(2)(5)}$	Data output disable time	Slave mode	TBD	TBD	
$t_{v(SO)}^{(2)(1)}$	Data output valid time	Slave mode (after enable edge)		TBD	
		$f_{PCLK} = \text{TBD}$		TBD	
$t_{v(MO)}^{(2)(1)}$	Data output valid time	Master mode (after enable edge)		TBD	
		$f_{PCLK} = \text{TBD}$	TBD	TBD	
$t_{h(SO)}^{(2)}$	Data output hold time	Slave mode (after enable edge)	TBD		
$t_{h(MO)}^{(2)}$		Master mode (after enable edge)	TBD		

1. TBD = to be determined.
2. Values based on design simulation and/or characterization results, and not tested in production.
3. Depends on  $f_{PCLK}$ . For example, if  $f_{PCLK} = 8\text{MHz}$ , then  $t_{PCLK} = 1/f_{PCLK} = 125\text{ ns}$  and  $t_{v(MO)} = 255\text{ ns}$ .
4. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
5. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z

Figure 19. SPI timing diagram - slave mode and CPHA = 0



1. Measurement points are done at CMOS levels:  $0.3V_{DD}$  and  $0.7V_{DD}$ .

Figure 20. SPI timing diagram - slave mode and CPHA = 1<sup>1)</sup>

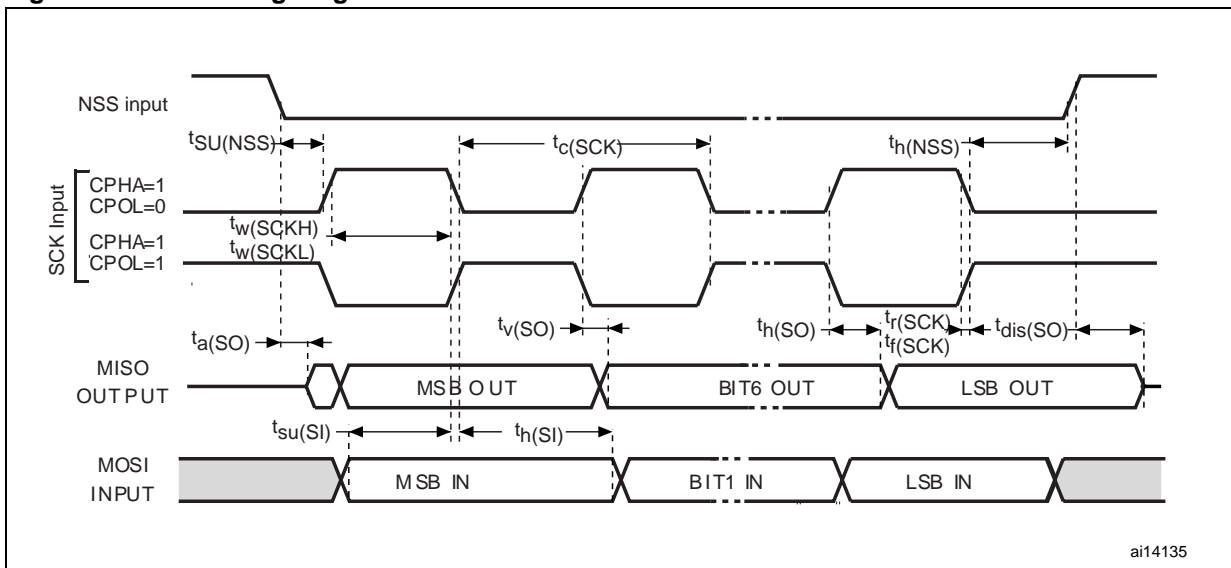
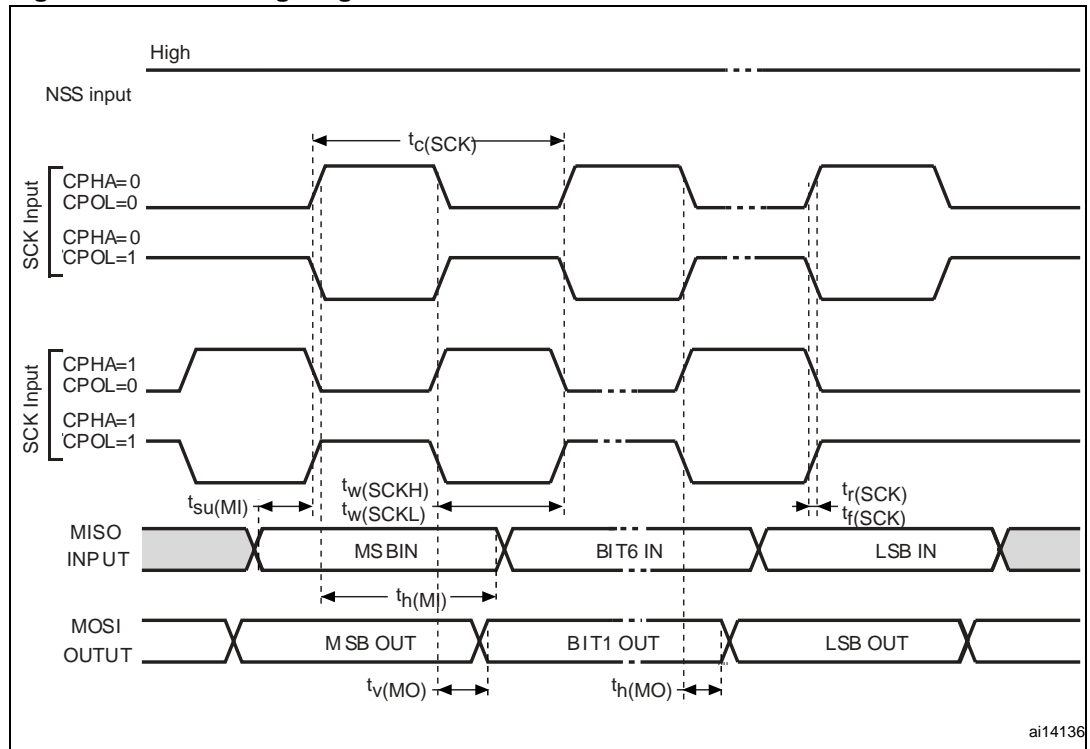


Figure 21. SPI timing diagram - master mode



1. Measurement points are done at CMOS levels:  $0.3V_{DD}$  and  $0.7V_{DD}$ .

**USB characteristics**

The USB interface is USB-IF certified (Full Speed).

Table 37. USB DC electrical characteristics

Symbol	Parameter	Conditions	Min. <sup>(1)</sup>	Max. <sup>(1)</sup>	Unit
<b>Input levels</b>					
$V_{DI}$	Differential input sensitivity	I(USB <sub>DP</sub> , USB <sub>DM</sub> )	0.2		V
$V_{CM}$	Differential common mode range	Includes $V_{DI}$ range	0.8	2.5	
$V_{SE}$	Single ended receiver threshold		1.3	2.0	
<b>Output levels</b>					
$V_{OL}$	Static output level low	$R_L$ of 1.5 k $\Omega$ to 3.6 V <sup>(2)</sup>		0.3	V
$V_{OH}$	Static output level high	$R_L$ of 15 k $\Omega$ to $V_{SS}$ <sup>(2)</sup>	2.8	3.6	

1. All the voltages are measured from the local ground potential.
2.  $R_L$  is the load connected on the USB drivers

Figure 22. USB timings: definition of data signal rise and fall time

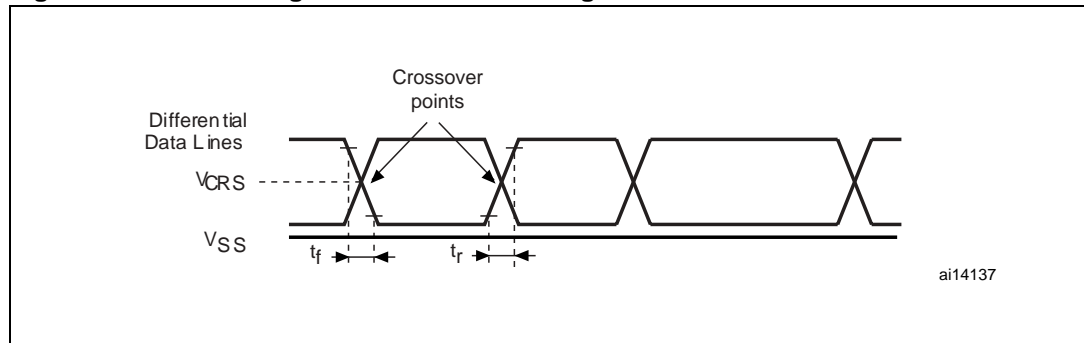


Table 38. USB: Full speed electrical characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
<b>Driver characteristics</b>					
$t_r$	Rise time <sup>(1)</sup>	$C_L = 50 \text{ pF}$	4	20	ns
$t_f$	Fall Time <sup>(1)</sup>	$C_L = 50 \text{ pF}$	4	20	ns
$t_{rfm}$	Rise/ fall time matching	$t_r/t_f$	90	110	%
$V_{CRS}$	Output signal crossover voltage		1.3	2.0	V

1. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).

### 5.3.16 CAN (controller area network) interface

Refer to I/O port characteristics for more details on the input/output alternate function characteristics (CANTX and CANRX).

### 5.3.17 12-bit ADC characteristics

Unless otherwise specified, the parameters given in [Table 39](#) are derived from tests performed under ambient temperature,  $f_{PCLK2}$  frequency and  $V_{DDA}$  supply voltage conditions summarized in [Table 7](#).

Note: It is recommended to perform a calibration after each power-up.

Table 39. ADC characteristics<sup>(1)</sup>

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DDA}$	ADC power supply		2.4V		3.6V	V
$V_{REF+}$	Positive reference voltage		2.0		$V_{DDA}$	V
$f_{ADC}$	ADC clock frequency		0.6		14	MHz
$f_S$	Sampling rate	TBD	0.05		1	MHz
$f_{TRIG}$	External trigger frequency	$f_{ADC} = 14 \text{ MHz}$			823	kHz
					17	$1/f_{ADC}$
$V_{AIN}$	Conversion voltage range <sup>(2)</sup>		$V_{SSA}$		$V_{DDA}$	V

**Table 39. ADC characteristics<sup>(1)</sup> (continued)**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R <sub>AIN</sub>	External input impedance		TBD <sup>(2)(3)</sup>			kΩ
C <sub>AIN</sub>	External capacitor on analog input					μF
I <sub>lkg</sub>	Negative input leakage current on analog pins	V <sub>IN</sub> < V <sub>SS</sub> ,  I <sub>IN</sub>   < 400 μA on adjacent analog pin		5	6	μA
R <sub>ADC</sub>	Sampling switch resistance				1	kΩ
C <sub>ADC</sub>	Internal sample and hold capacitor				5	pF
t <sub>CAL</sub>	Calibration time	f <sub>ADC</sub> = 14MHz	5.9			μs
			83			1/f <sub>ADC</sub>
t <sub>lat</sub>	Injection conversion latency	f <sub>ADC</sub> = 14 MHz			0.214	μs
					3	1/f <sub>ADC</sub>
t <sub>S</sub>	Sampling time	f <sub>ADC</sub> = 14 MHz	0.107		17.1	μs
t <sub>STAB</sub>	Power-up time		0	0	1	μs
t <sub>CONV</sub>	Total conversion time (including sampling time)	f <sub>ADC</sub> = 14 MHz	1		18	μs
			14 (1.5 for sampling +12.5 for successive approximation)			1/f <sub>ADC</sub>

1. TBD = to be determined.
2. Depending on the input signal variation (f<sub>AIN</sub>), C<sub>AIN</sub> can be increased for stabilization time and reduced to allow the use of a larger serial resistor (R<sub>AIN</sub>). It is valid for all f<sub>ADC</sub> frequencies ≤14 MHz.
3. During the sample time the input capacitance C<sub>AIN</sub> (5 max) can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t<sub>S</sub>. After the end of the sample time t<sub>S</sub>, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t<sub>S</sub> depend on programming.

**Table 40. ADC accuracy (f<sub>PCLK2</sub> = 14 MHz, f<sub>ADC</sub> = 14 MHz, R<sub>AIN</sub> <10 kΩ, V<sub>DDA</sub> = 3.3 V)<sup>(1)</sup>**

Symbol	Parameter	Conditions	Typ	Max	Unit
E <sub>T</sub>	Total unadjusted error <sup>(2)</sup>		3	TBD	LSB
E <sub>O</sub>	Offset error <sup>(2)</sup>		1	TBD	
E <sub>G</sub>	Gain Error <sup>(2)</sup>		2	TBD	
E <sub>D</sub>	Differential linearity error <sup>(2)</sup>		3	TBD	
E <sub>L</sub>	Integral linearity error <sup>(2)</sup>		2	TBD	

1. TBD = to be determined.
2. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for I<sub>INJ(PIN)</sub> and ΣI<sub>INJ(PIN)</sub> in [Section 5.3.12](#) does not affect the ADC accuracy.

Figure 23. ADC accuracy characteristics

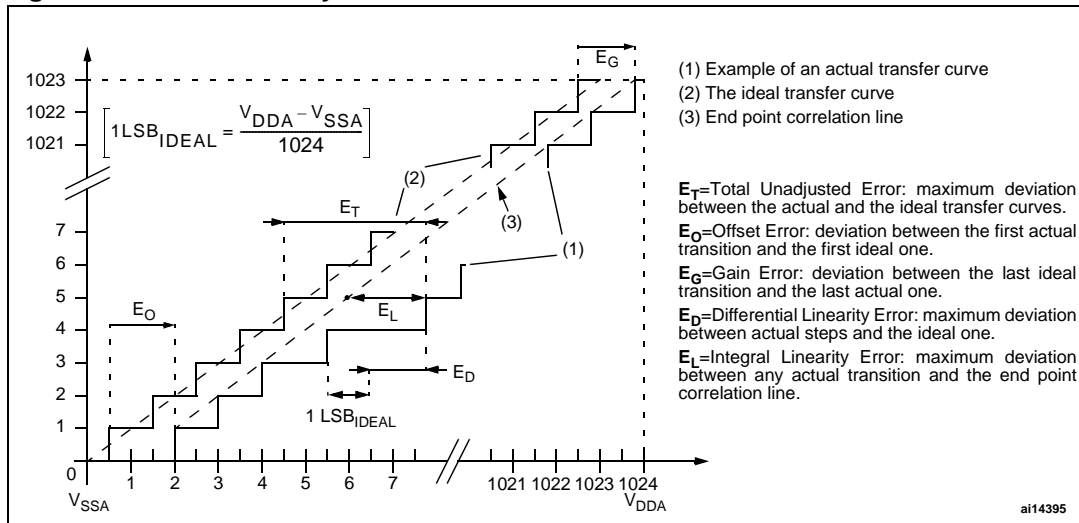
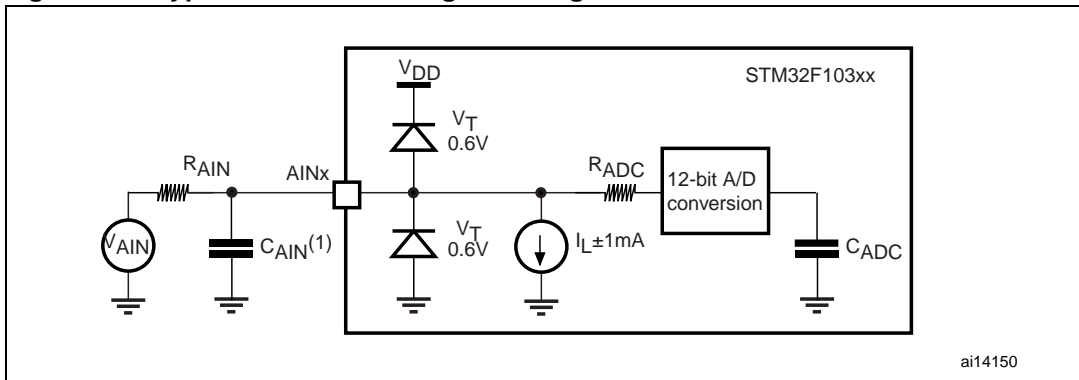


Figure 24. Typical connection diagram using the ADC



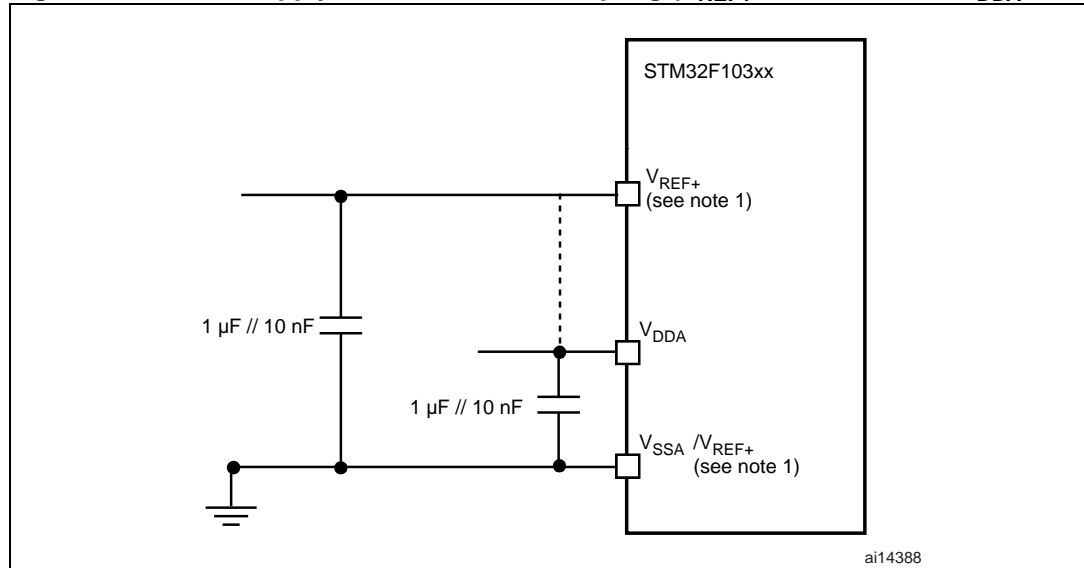
1. Refer to [Table 39](#) for the values of  $R_{ADC}$  and  $C_{ADC}$ .
2.  $C_{PARASITIC}$  must be added to  $C_{AIN}$ . It represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (3 pF). A high  $C_{PARASITIC}$  value will downgrade conversion accuracy. To remedy this,  $f_{ADC}$  should be reduced.



**General PCB design guidelines**

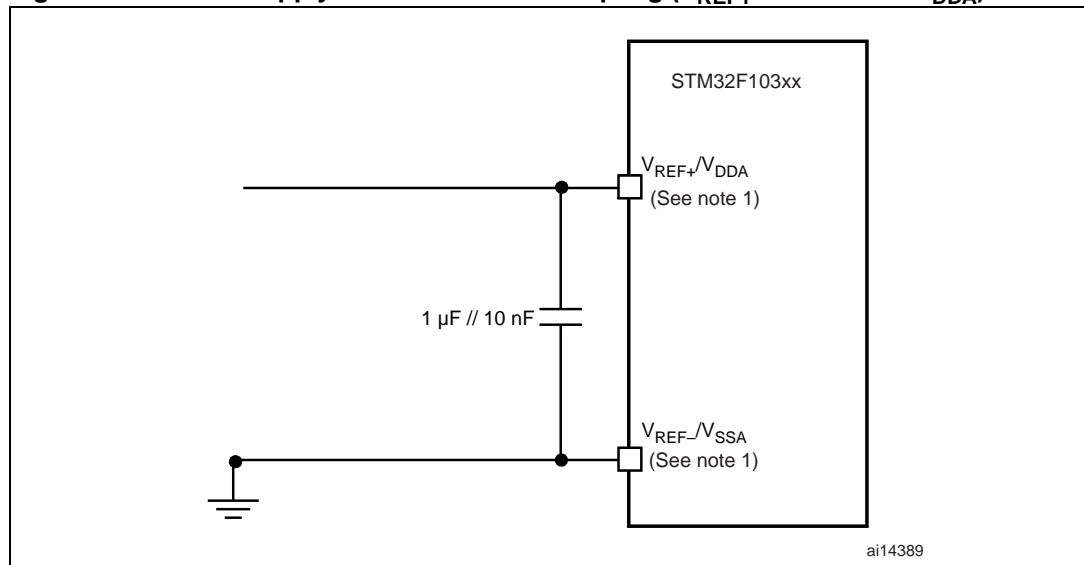
Power supply decoupling should be performed as shown in [Figure 25](#) or [Figure 26](#), depending on whether  $V_{REF+}$  is connected to  $V_{DDA}$  or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

**Figure 25. Power supply and reference decoupling ( $V_{REF+}$  not connected to  $V_{DDA}$ )**



1.  $V_{REF+}$  and  $V_{REF-}$  inputs are available only on 100-pin packages.

**Figure 26. Power supply and reference decoupling ( $V_{REF+}$  connected to  $V_{DDA}$ )**



1.  $V_{REF+}$  and  $V_{REF-}$  inputs are available only on 100-pin packages.

### 5.3.18 Temperature sensor characteristics

**Table 41. TS characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_L$	$V_{SENSE}$ linearity with temperature			$\pm 1.5$		°C
Avg_Slope	Average slope			4.478		mV/°C
$V_{25}$	Voltage at 25 °C			1.4		V
$t_{START}$	Startup time		4		10	$\mu s$

## 6 Package characteristics

Figure 27. LFBGA100 - low profile fine pitch ball grid array package outline

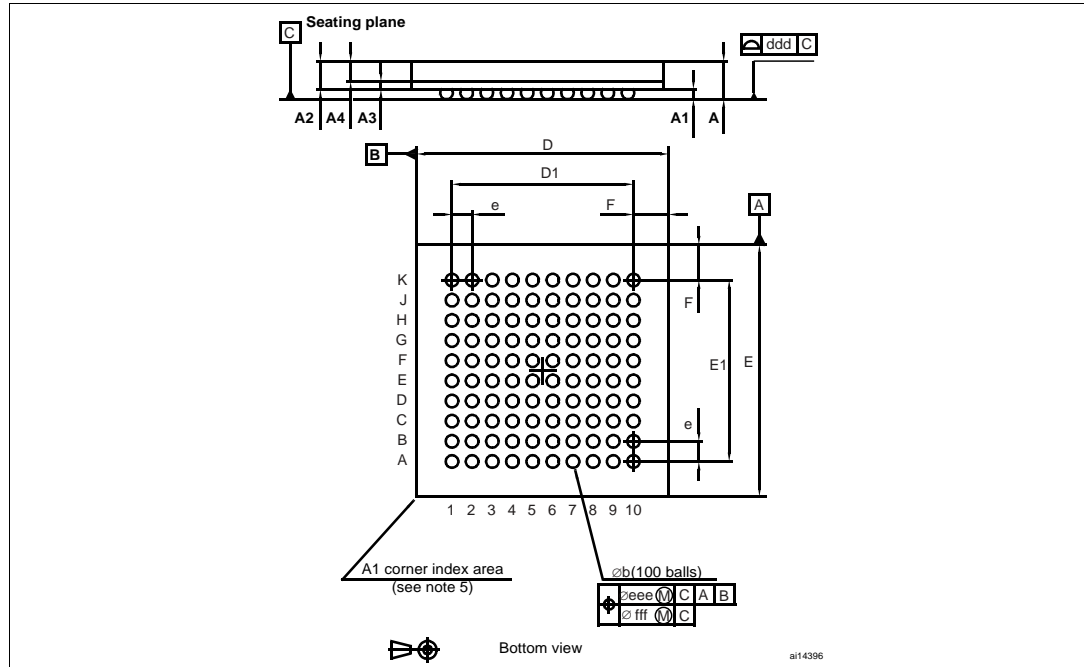


Table 42. LFBGA100 - low profile fine pitch ball grid array package mechanical data

Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			1.700			0.067
A1	0.270			0.011		
A2		1.085			0.043	
A3		0.30			0.012	
A4			0.80			0.031
b	0.45	0.50	0.55	0.018	0.020	0.022
D	9.85	10.00	10.15	0.388	0.394	0.40
D1		7.20			0.283	
E	9.85	10.00	10.15	0.388	0.394	0.40
E1		7.20			0.283	
e		0.80			0.031	
F		1.40			0.055	
ddd			0.12			0.005
eee			0.15			0.006
fff			0.08			0.003
N (number of balls)	100					

**Figure 28. Recommended PCB design rules (0.80/0.75 mm pitch BGA)**

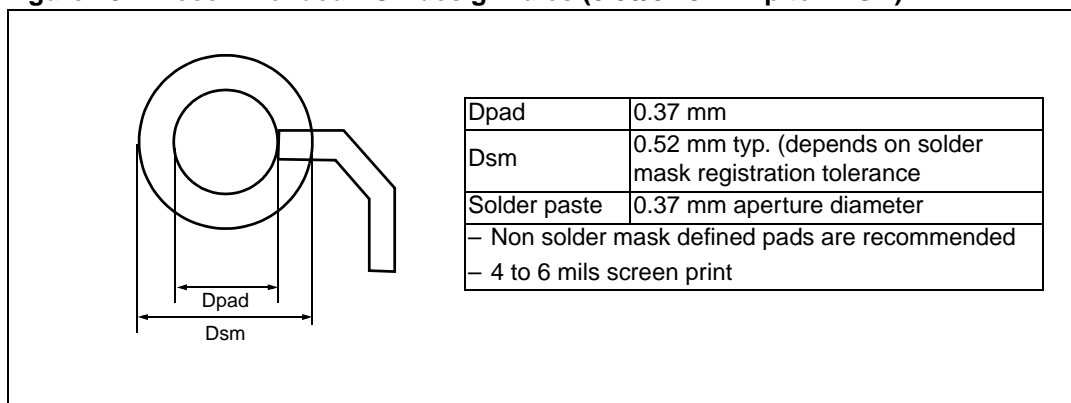


Figure 29. LQFP100 – 100-pin low-profile quad flat package outline

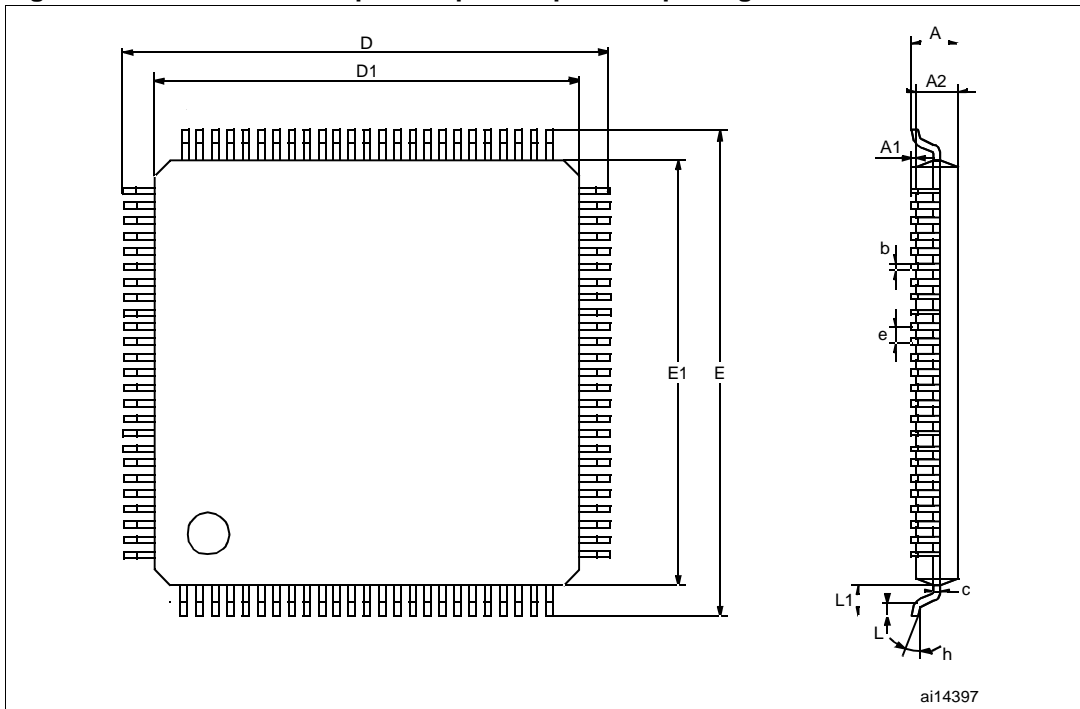


Table 43. LQFP100 – 100-pin low-profile quad flat package mechanical data

Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
C	0.09		0.20	0.004		0.008
D		16.00			0.630	
D1		14.00			0.551	
E		16.00			0.630	
E1		14.00			0.551	
e		0.50			0.020	
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
	<b>Number of pins</b>					
N	100					

Figure 30. LQFP64 – 64 pin low-profile quad flat package outline

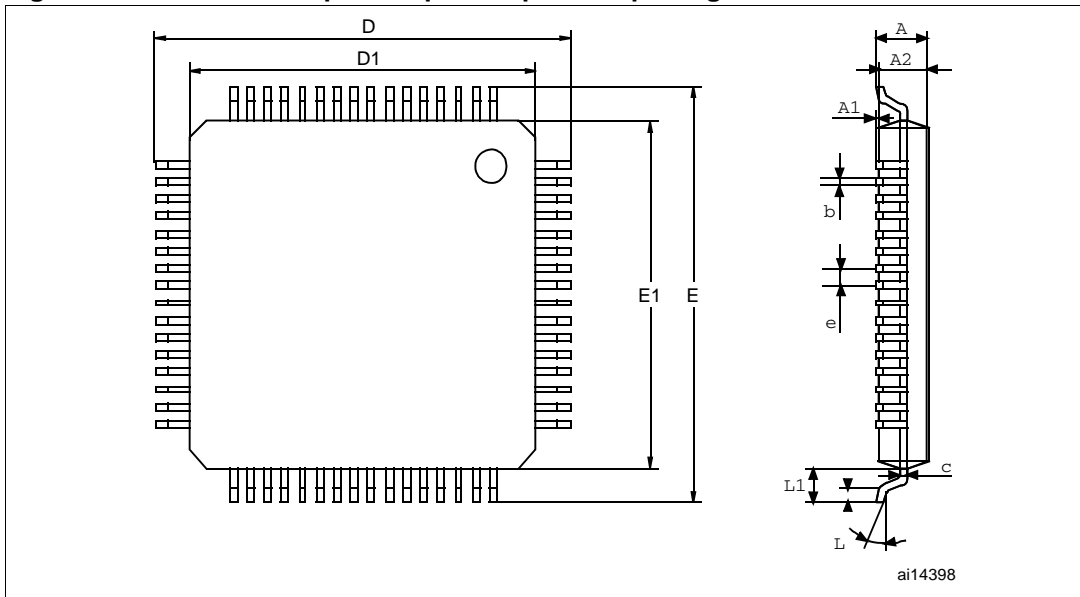


Table 44. LQFP64 – 64 pin low-profile quad flat package mechanical data

Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.09		0.20	0.004		0.008
D		12.00			0.472	
D1		10.00			0.394	
E		12.00			0.472	
E1		10.00			0.394	
e		0.50			0.020	
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
	<b>Number of pins</b>					
N	64					

Figure 31. LQFP48 – 48 pin low-profile quad flat package outline

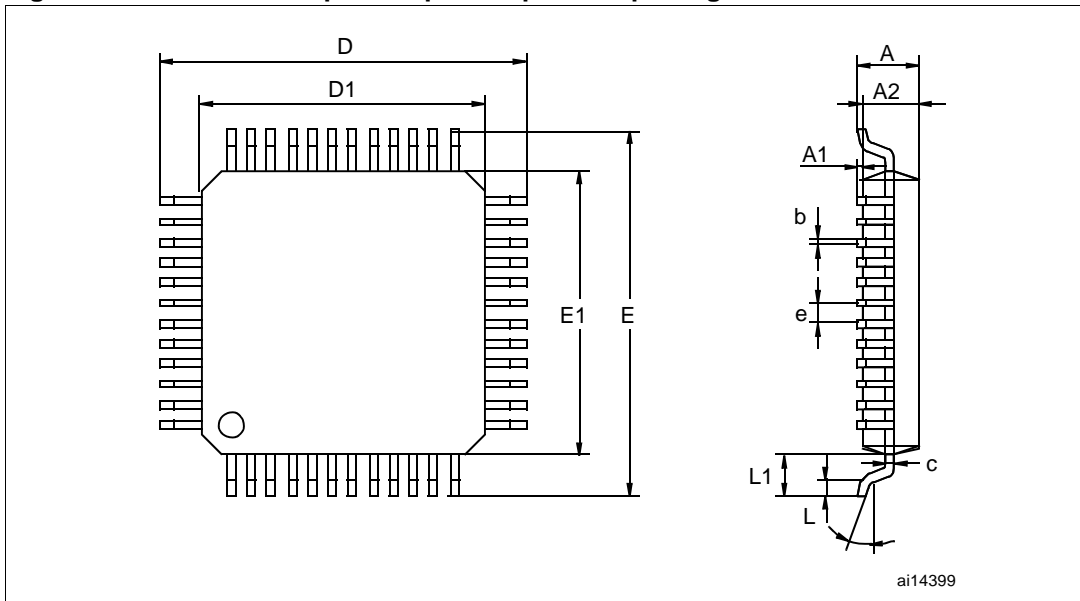


Table 45. LQFP48 – 48 pin low-profile quad flat package mechanical data

Dim.	mm			inches <sup>(1)</sup>		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
C	0.09		0.20	0.004		0.008
D		9.00			0.354	
D1		7.00			0.276	
E		9.00			0.354	
E1		7.00			0.276	
e		0.50			0.020	
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
	<b>Number of pins</b>					
N	48					

1. Values in inches are converted from mm and rounded to 3 decimal digits.

## 6.1 Thermal characteristics

The average chip-junction temperature,  $T_J$ , in degrees Celsius, may be calculated using the following equation:

$$T_J = T_A + (P_D \times \Theta_{JA}) \tag{1}$$

Where:

- $T_A$  is the Ambient Temperature in °C,
- $\Theta_{JA}$  is the Package Junction-to-Ambient Thermal Resistance, in °C/W,
- $P_D$  is the sum of  $P_{INT}$  and  $P_{I/O}$  ( $P_D = P_{INT} + P_{I/O}$ ),
- $P_{INT}$  is the product of  $I_{DD}$  and  $V_{DD}$ , expressed in Watts. This is the Chip Internal Power.

$P_{I/O}$  represents the Power Dissipation on Input and Output Pins;

Most of the time for the application  $P_{I/O} < P_{INT}$  and can be neglected. On the other hand,  $P_{I/O}$  may be significant if the device is configured to drive continuously external modules and/or memories.

An approximate relationship between  $P_D$  and  $T_J$  (if  $P_{I/O}$  is neglected) is given by:

$$P_D = K / (T_J + 273 \text{ °C}) \tag{2}$$

Therefore (solving equations 1 and 2):

$$K = P_D \times (T_A + 273\text{°C}) + \Theta_{JA} \times P_D^2 \tag{3}$$

where:

K is a constant for the particular part, which may be determined from equation (3) by measuring  $P_D$  (at equilibrium) for a known  $T_A$ . Using this value of K, the values of  $P_D$  and  $T_J$  may be obtained by solving equations (1) and (2) iteratively for any value of  $T_A$ .

**Table 46. Thermal characteristics**

Symbol	Parameter	Value	Unit
$\Theta_{JA}$	<b>Thermal resistance junction-ambient</b> LFBGA100 - 10 x 10 mm / 0.5 mm pitch	41	°C/W
	<b>Thermal resistance junction-ambient</b> LQFP100 - 14 x 14 mm / 0.5 mm pitch	46	
	<b>Thermal Resistance Junction-Ambient</b> LQFP64 - 10 x 10 mm / 0.5 mm pitch	45	
	<b>Thermal resistance junction-ambient</b> LQFP48 - 7 x 7 mm / 0.5 mm pitch	55	



## 7 Order codes

Table 47. Order codes

Part number	Flash program memory Kbytes	SRAM memory Kbytes	Package
STM32F103C6T6	32	10	LQFP48
STM32F103C8T6	64	20	
STM32F103R6T6	32	10	LQFP64
STM32F103R8T6	64	20	
STM32F103RBT6	128	20	
STM32F103V8T6	64	20	LQFP100
STM32F103VBT6	128	20	
STM32F103V8H6	64	20	LFBGA100
STM32F103VBH6	128	20	

### 7.1 Future family enhancements

Further developments of the STM32F103xx performance line will see an expansion of the current options. Larger packages will soon be available with up to 512KB Flash, 64KB SRAM and with extended features such as EMI support, SDIO, I2S, DAC and additional timers and USARTS.

## 8 Revision history

**Table 48. Document revision history**

Date	Revision	Changes
01-jun-2007	1	Initial release.
20-Jul-2007	2	<p>Flash memory size modified in <a href="#">Note 5</a>, <a href="#">Note 4</a>, <a href="#">Note 6</a>, <a href="#">Note 7</a> and BGA100 pins added to <a href="#">Table 3: Pin definitions</a>. <a href="#">Figure 5: STM32F103xx performance line BGA100 ballout</a> added.</p> <p><math>T_{HSE}</math> changed to <math>T_{LSE}</math> in <a href="#">Figure 12: Low-speed external clock source AC timing diagram</a>. <math>V_{BAT}</math> ranged modified in <a href="#">Power supply schemes</a>.</p> <p><math>t_{SU(LSE)}</math> changed to <math>t_{SU(HSE)}</math> in <a href="#">Table 17: HSE 4-16 MHz oscillator characteristics</a>. <math>I_{DD(HSI)}</math> max value added to <a href="#">Table 19: HSI oscillator characteristics</a>.</p> <p>Sample size modified and machine model removed in <a href="#">Electrostatic discharge (ESD)</a>.</p> <p>Number of parts modified and standard reference updated in <a href="#">Static latch-up</a>. 25 °C and 85 °C conditions removed and class name modified in <a href="#">Table 28: Electrical sensitivities</a>. <math>R_{PU}</math> and <math>R_{PD}</math> min and max values added to <a href="#">Table 29: I/O static characteristics</a>. <math>R_{PU}</math> min and max values added to <a href="#">Table 32: NRST pin characteristics</a>.</p> <p><a href="#">Figure 18: I<sup>2</sup>C bus AC waveforms and measurement circuit</a> and <a href="#">Figure 17: Recommended NRST pin protection</a> corrected.</p> <p>Notes removed below <a href="#">Table 7</a>, <a href="#">Table 32</a>, <a href="#">Table 37</a>.</p> <p><math>I_{DD}</math> typical values changed in <a href="#">Table 11: Maximum current consumption in Run and Sleep modes</a>. <a href="#">Table 33: TIMx characteristics</a> modified.</p> <p><math>t_{STAB}</math>, <math>V_{REF+}</math> value, <math>t_{lat}</math> and <math>f_{TRIG}</math> added to <a href="#">Table 39: ADC characteristics</a>. In <a href="#">Table 24: Flash memory endurance and data retention</a>, typical endurance and data retention for <math>T_A = 85</math> °C added, data retention for <math>T_A = 25</math> °C removed.</p> <p><math>V_{BG}</math> changed to <math>V_{REFINT}</math> in <a href="#">Table 10: Embedded internal reference voltage</a>. Document title changed. <a href="#">Controller area network (CAN)</a> section modified.</p> <p><a href="#">Figure 9: Power supply scheme</a> modified.</p> <p><a href="#">Features on page 1</a> list optimized. Small text changes.</p>

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